Temporary Pixel-planes Interfaces

1. Masscomp MULTIBUS Memory Map

The table below specifies the memory map of the Pixel-planes modules on the Masscomp MULTIBUS. The IGC MULTIBUS interface and Translator occupy the same memory locations because only one or the other will be used at any one time. Modification of the VC and the Translator is necessary to accomodate the 24 bit addressing used on the Masscomp addressing instead of 20 bit addressing on the Pixel-planes MULTIBUS. The address of the modules will be different on on the Pixel-planes MULTIBUS due to the fewer number of address bits.

Address (Hex)	Words (Decimal)	Bits	Description
FB0000	*4096*	*⟨0:7⟩*	*VC Vertical Sync Control*
FB1000	*2048*	*⟨0:15⟩*	*VC Red and Green Video Test Memory*
FB1800	*2048*	*⟨0:15⟩*	*VC Blue and Extra Video Test Memory*
FB2000	*2048*	*⟨0:15⟩*	*VC Video Train Control*
FB2800	*256*	*⟨0:7⟩*	*VC Red Color Lookup Table*
FB2900	*256*	*⟨0:7⟩*	*VC Green Color Lookup Table*
FB2A00	*256*	*⟨0:7⟩*	*VC Blue Color Lookup Table*
FB2B08	*256*	*⟨0:7⟩*	*VC Horizontal Sync Control*
FB2C00	*1*	*⟨0:15⟩*	*VC ScanIn Data Register*
FB2D00	*1*	*⟨0:15⟩*	*VC ScanOut Data Register*
FB2E00	*1*	*⟨0:8⟩*	*VC Control Register*
FB2F00	*tbd*	*⟨0:15⟩*	*Translator Registers*
FB2F00	*16*	*⟨0:15⟩*	*IGC MULTIBUS Interface*

2. Software Interface

The format of the Pixel-planes read and write subroutine calls will be identical for both the temporary and permanent versions so that the physical location of the boards will be transparant to the user. Recompilation with the different driver and different addresses is all that is necessary to change versions.

The format of the subroutine calls is as follows:

```
ppwrite(SrcAddress, DestAddress, WordCount)
short   *SrcAddress;    /* pointer to the first 16 bit data word in main  */
                        /* memory that is to be transferred  */
short   *DestAddress;   /* pointer to the first memory location on the  */
                        /* pixel-planes MULTIBUS or Masscomp MULTIBUS */
                        /* to which the data is transferred  */
int     WordCount;      /* number of 16 bit words to be transferred  */


ppread(SrcAddress, DestAddress, WordCount)
short   *SrcAddress;    /* pointer to the first 16 bit word location in */
                        /* main memory to which the data is transferred */
short   *DestAddress;   /* pointer to the first memory location on the  */
```

```
                    /* Pixel-planes MULTIBUS or Masscomp MULTIBUS */
                    /* from which the data is transferred */
int     WordCount;  /* number of 16 bit words to be transferred */
```

3. Description of the Temporary IGC MULTIBUS Interface

The temporary IGC MULTIBUS interface consists of 16 write only registers, beginning at Masscomp backplane address 0xFB2F00 and one read only register located at Masscomp backplane address 0xFB2F00.

The write only registers are arranged as pairs, the even address containing the 16 LSBs of the IGC data word, and the odd address containing the 16 MSBs of the IGC data word. The address of the register determines the type of word that is sent to the IGC. For example, to send word type 101, the 16 LSBs of data must be written to address 0xFB000A, and the 16 MSBs of data must be written to address 0xFB000B. The IGC write enable signal is generated to the IGC when the even address is written, so the LSBs of the data word must be written before the MSBs.

The read only register contains a status bit that indicates whether the IGC is able to accept another word or is busy. The busy condition can only occur after writing an I-word (instruction bits set to 011). It is the responsibility of the user software to not write another word until the IGC is no longer busy. This check can be made immediately after writing the command, or prior to writing the next command. The other bits of this read only register are undetermined, so the LSB should be masked before checking.