2.5 Video Controller — DRAFT

This document defines the interfaces between the *Video Controller* (VC) and the other *Pixel-Planes* subsystems, specifies the VC hardware, and describes each function of the VC. The interface definition is a subset of the data found in section 1.2. The hardware specification describes the operation of each of the five VC modules. The functional description describes the host software requirements, the interaction of the different hardware modules, and the microcode in each VC module required to perform each function.

2.5.1 Interfaces

2.5.1.1 MULTIBUS Interface

The VC interfaces to the MULTIBUS signals described in section 1.2. Microcode memory, video scan memory, a control register, and scan data input and output registers are located at the MULTIBUS memory locations specified in Figure 2.5.1. The specific control register bit assignments are described in section 2.5.2.1. Approximately 4K address space is reserved for future expansion.

2.5.1.2 Video Train Interface

The video train signals are described in Figure 2.5.2. The leading **"B"** in the signal name indicates an intraboard signal, most of which interface to the *Pixel-Planes* chip through buffers, producing the root signal name directly at the *Pixel-Planes* chip interface. The remaining signals interface only to the video train control logic. The eight bits of "extra" video data are provided for future expansion to high resolution display and are not implemented in this version of *Pixel-Planes*.

2.5.1.3 CRT Interface

The VC outputs RGB composite analog video data. The interface shall present a 75 ohm load to the VC.

2.5.1.4 Image Generation Controller Interface

The signal **VRBHLXF**, P2-tbd, is output to the Image Generation Controller to indicate the beginning of vertical retrace. The signal is high for a *tbd* period beginning *tbd* after the beginning of the vertical blanking signal.

2.5.2 Video Hardware Specification

A block diagram of the Video hardware is shown in Figure 2.5.3. This section describes the five VC modules: MULTIBUS Interface, Clock Generation, Sync Generation, Pixel Control, and Video Output. The schematic diagrams for each module are contained in Appendix A.

2.5.2.1 MULTIBUS Interface

The MULTIBUS interface buffers the MULTIBUS signals, decodes the appropriate addresses, generates the **XACK*** signal, contains the VC control register, and the ScanIn and ScanOut data registers.

All signals on the MULTIBUS interface directly to 74S240 inverting bus drivers and receivers. The 20 address bits are decoded and chip selects and read enables for registers and memories are routed to the appropriate module.

The MULTIBUS to microcode enable bit, **MBMCEnaH**, in the control register enables the chip selects, address, and data to the microcode memory. When an address in the microcode memory address range is generated, the **XACK*** signal is immediately generated (whether or not **MBMCEnaH** is set).

Address	Words	Bits	Description
x	*4096*	*⟨0:7⟩*	*Vertical Sync Control*
x+4k	*2048*	*⟨0:15⟩*	*Red and Green Video Test Memory*
x+6k	*2048*	*⟨0:15⟩*	*Blue and Extra Video Test Memory*
x+8k	*2048*	*⟨0:15⟩*	*Video Train Control*
x+10k	*256*	*⟨0:7⟩*	*Red Color Lookup Table*
x+10k+256	*256*	*⟨0:7⟩*	*Green Color Lookup Table*
x+10k+512	*256*	*⟨0:7⟩*	*Blue Color Lookup Table*
x+10k+768	*256*	*⟨0:7⟩*	*Horizontal Sync Control*
x+11k	*1*	*⟨0:15⟩*	*ScanIn Data Register*
x+11k+256	*1*	*⟨0:15⟩*	*ScanOut Data Register*
x+11k+512k	*1*	*⟨0:8⟩*	*Control Register*
x+11k+768	*256*		*Future Use*
x+12k	*4096*		*Future Use*

Figure 2.5.1: Video Controller MULTIBUS Memory Locations.

Pin	Signal Name	Description
P2-tbd	*Px*	*Video Data Video Clock*
P2-tbd	*V*	*Video Data Shift Clock*
J3-tbd	*BRed⟨0:7⟩HLVR*	*Red Video Data*
J3-tbd	*BBlue⟨0:7⟩HLVR*	*Blue Video Data*
J3-tbd	*BGreen⟨0:7⟩HLVR*	*Green Video Data*
J3-tbd	*BExtra⟨0:7⟩HLVR*	*Extra Video Data*
P2-tbd	*BPAdd⟨0:4⟩LLXF*	*Pixel address on a logical chip*
P2-tbd	*BBAdd⟨0:3⟩LLXF*	*Byte address at a pixel*
P2-tbd	*BShdLdLLXF*	*Shadow-Register unload control*
P2-tbd	*BScShLLXF*	*Scan path shift enable*
P2-tbd	*BScCnt⟨0:1⟩LLXF*	*Scan path function control*
J2-tbd	*BScInHLXR*	*Scan path input*
J3-tbd	*BScOutLLXF*	*Scan path output*
P2-tbd	*BRLdLLXF*	*Red Video register load*
P2-tbd	*BGLdLLXF*	*Green Video register load*
P2-tbd	*BBLdLLXF*	*Blue Video register load*
P2-tbd	*BELdLLXF*	*Extra Video register load*
P2-tbd	*BLBdEnaLLVR*	*Video train register select*
P2-tbd	*BLBdEnaHLVR*	*Video train register select*

Figure 2.5.2: Video Train Interface Signals

The bit specification for the control register is shown in Figure 2.5.4. The control register bits select options in the different VC modules, and their function is described in that module's section. If a control register address is selected, the **XACK*** signal is immediately generated.

The ScanIn register stores data that is to be shifted into the **ScInHLXR** input of the *Pixel-Planes* array. The ScanOut register stores data that is shifted out of the **ScOutHLXR** output of the *Pixel-Planes* array.

Block Diagram of Video Controller

Figure 2.5.3: Video Controller Block Diagram.

When the ScanIn register is selected, data on the MULTIBUS is loaded into the shift register. After the register is loaded, the **ScShHLXR** signal is generated for 16 clock cycles and the data is shifted into the array. Simultaneously, data from the ScOutHEXR bit is shifted into the ScanOut register. After 16 **Px** clock cycles, **ScShHLXR** is removed, the shifting process is disabled, and the **XACK*** signal is generated.

The proper scan path must be selected by setting the **ScCnt⟨0:1⟩HLXR** bits to 00, 01, or 10 before data is shifted into the array. The **Px** clock signal should be set to the **CCLK*/4** signal to prevent synchronization failures. The **XACK*** signal will be generated whether or not these two setup steps have occurred.

When the Scanout register is selected, the data in the Scanout register is enabled onto the MULTIBUS and the **XACK*** signal is generated. This action assumes that valid data has been shifted into the register by a previous write to the ScanIn register as described in the previous paragraph.

2.5.2.2 Clock Generation

The Clock Generation module generates true and inverted **V**, **Px** and **VMux** clock signals. The frequency of these clocks is selected by the **VSel⟨0:1⟩HLXR** and **PxSel⟨0:1⟩HLXR** bits in the control register (see Figure 2.5.4) and, if selected, the external oscillator input. The internal oscillator frequency is 32 MHz. This speed will be sufficient for all display sizes to 512 x 512 noninterlaced 60 Hz. The external oscillator input allows a higher frequency oscillator for 1024 x 1024 displays, or an alternate frequency that would allow precise screen area filling by the display. Alternatively, the present oscillator could be replaced by the higher frequency oscillator.

The **InOscSelL** bit selects the internal oscillator when low and the external oscillator when high. The **VSel⟨0:1⟩HLXR** bits select the **V** clock rate to be 1/2, 1/4, or 1/8 the frequency of

Bit	Signal Name	Description
0	*InOscSelL*	*Oscillator Select:* *0: Internal* *1: External*
⟨1:2⟩	*PxSel⟨0:1⟩*	*Px Clock Rate Select:* *00: Osc/8* *01: Osc/16* *10: Osc/32* *11: CCLK*/4*
⟨3:4⟩	*VSel⟨0:1⟩*	*V Clock Rate Select:* *00: Osc/2* *01: Osc/4* *10: Osc/8* *11: SlowVHLXR*
5	*LoResEnL*	*Low Resolution Enable:* *0: Low Resolution* *1: High Resolution*
6	*MBMCEnaH*	*MULTIBUS Microcode Enable:* *0: Disable MULTIBUS access* *1: Enable MULTIBUS access*
⟨7:8⟩	*ScCnt⟨0:1⟩*	*Scan Path Select:* *00: ScanIn to ScanOut* *01: Through Alive Register* *10: Through X-Y Register* *11: Through Global Token Register*

Figure 2.5.4: Control Register Bit Assignments.

the selected oscillator, or **SlowVHLXR**. **SlowVHLXR** is a microcode bit in the Video Train microcode. The **PxSel⟨0:1⟩HLXR** bits select the **Px** clock to be 1/8, 1/16, or 1/32 the frequency of the selected oscillator, or 1/4 of the **CCLK*** frequency. Selection of the proper combination of **V** and **Px** clock frequencies is discussed in section 2.5.3.1.

The video mux clock, **VMux**, will be used for high resolution display in later versions of *Pixel-Planes*.

2.5.2.3 Video Sync Generation

This module generates the video synchronization and blanking signals required for video output, as well as control bits required by the Video Train microcode.

The horizontal pixel counter counts **Px** clock cycles to determine the length of one raster line. The outputs of the counter address a 256 x 8 microcode RAM, which outputs 6 control and synchronization signals. The description of each of the six bits is shown in Figure 2.5.5. The RAM data outputs are latched on the falling edge of **Px** clock.

The RAM address and control inputs, and data inputs and outputs are multiplexed to allow the RAM to be written and read from the MULTIBUS. The **MBMCEnaH** bit in the control register must be low during display to allow generation of the sync signals, and high to allow MULTIBUS access to the RAM.

The vertical raster counter counts the number of half-raster lines. It is enabled by the **HLHEXF** bit, which is high for one **Px** clock cycle at the middle and one **Px** clock cycle at the end of each horizontal line. The outputs of the counter address a 2048 x 8 microcode RAM, which

Bit	Signal Name	Description
0	*HSyncLLXF*	*Normal Horizontal Sync*
1	*HSerLLXF*	*Serrated Horizontal Sync*
2	*HEqlLLXF*	*Equalized Horizontal Sync*
3	*HBlnkHLXF*	*Horizontal Blank*
4	*EoLLEXF*	*End of Horizontal Line*
5	*HLHEXF*	*Half Horizontal Line Enable*

Figure 2.5.5: Horizontal Sync Microcode Bits.

Bit	Signal Name	Description
⟨*0:1*⟩	*HSySl⟨0:1⟩*	*Select Horizontal Sync:* *00: Normal Sync* *01: Serration* *10: Equalization* *11: Not Used*
2	*VBlankHLXF*	*Vertical Blank*
⟨*3:5*⟩	*VTCnt⟨0:2⟩*	*Video Train Control:* *000: Normal Display* *001: Disable Display* *010: Even Retrace 1st Line Display* *011: Odd Retrace 1st Line Normal Display* *100: Pixel Address Increment Display* *101: New Pxpl Chip Display* *110: future use* *111: future use*
6	*EofFsLEXF*	*End of Fields*
7	*VRBHLXF*	*Vertical Retrace Begin*

Figure 2.5.6: Vertical Sync Microcode Bits.

stores the sequence of bits required for 8 signals during each field for noninterlaced display and for two fields for interlaced display. The description of each of the eight bits is shown in Figure 2.5.6. The RAM data outputs are latched on the falling edge of **Px** clock. The two **HSySel⟨0:1⟩HLXF** bits select either the normal horizontal sync, the serrated pulses, or the equalizing pulses from the horizontal microcode RAM. The **VTCnt⟨0:2⟩HEXF** control signals select the proper video train signals from the video train microcode RAM. The **EoFSLEXF** signal resets the vertical counter at the end of the second field in interlaced display and at the end of each field in noninterlaced display. The **VRBHLXF** signal is used by the IGC.

The RAM address and control inputs, and data inputs and outputs are multiplexed to allow the RAM to be written and read from the MULTIBUS. The **MBMCEnaH** bit in the control register must be low during display to allow generation of the sync signals, and high to allow MULTIBUS access to the RAM.

2.5.2.4 Pixel Control

The Pixel Control module generates video train and pixel plane chip control signals required to access the video data in the *Pixel-Planes* chips.

The eight address bits from the horizontal syncronization microcode RAM and the 3 video train control signals generated by the vertical line microcode RAM are used to address a 2048 x 16 microcode RAM. Each 256 location segment of the RAM stores the control signals for an entire scan line as selected by the horizontal address count. The eight segments each store different control signal patterns used during the field, and are selected by the **VTCnt(0:2)HEXF** bits.

The normal segment is used during most scan lines where no additional processing is required. The disable segment is used during all but the last scan line that is blanked during vertical retrace. The odd and even segments are used during the first active scan line of the odd or even field to generate a pixel address for the first or second line, and to preset the global token or move it to the center of the scan line. The pixel address increment segment is used during scan lines where the pixel address counter must be incremented. The new pxpl segment is used when, during the active field, the pixel address reaches the 64th line and must be reset to zero for the next scan line.

The address, data, and control lines are multiplexed so that the RAM can be read and written from the MULTIBUS.

2.5.2.5 Video Output

The Video Output module accepts the RGB digital data from the Video Train and generates the analog RGB outputs. In later versions of *Pixel-Planes* it will multiplex the RGB data along with the eight bits of extra data onto a high resolution signal for 1024 x 1024 displays.

The **LoResEnL** signal selects either the RGB data path for low resolution display, or the multiplexed data path. The 8 bit multiplexed data path directs 3 bits to the red and green looup tables, and 2 bits to the blue lookup tables. The **VMux** clock signal controls the high speed video mux in high resolution mode.

A hybrid circuit manufactured by Intech is used to output the RGB analog data. This part includes a 256 x 8 color lookup table for each of the RGB data.

The video scan memory is also included in this module. This memory is 2048 x 32 bits, and is used to store data as it is scanned out of the *Pixel-Planes* chips. The memory cannot run at the maximum speed of the video train, but is designed run at **V** clock rates that are less than the **Px** clock rate.

2.5.3 Functional Requirements

This section describes the functions that the Video Controller must perform. The VC must participate in the initialization of the *Pixel-Planes* array and control the scanout of video data from the array, producing the analog RGB signals to drive a CRT.

The prototype version of *Pixel-Planes* will have a 64 x 64 pixel array arranged as 4 logical boards of 16 logical chips each, and generate output for a 525 line interlaced monitor that will be driven 262 lines noninterlaced.

This section discusses how the host computer commands the VC, as well as the microcode required in each of the modules to perform these functions. The procedures are detailed for the 64 x 64 array, but included are the features and limitations that must be observed when setting up the VC for other array sizes.

2.5.3.1 Px Clock Generation

The VC generates the **Px** clock signal for the *Pixel-Planes* chips and the **V** clock signal for the video train. **Px** shall be 4 MHz during display, and synchronized to the MULTIBUS **CCLK*** whenever the ScanOut register is accessed. For smaller display sizes this clock may run at a slower rate if desired. The **Px** clock is not synchronized to the **Ph** clock.

The selection of the **V** clock rate is dependant on the CRT monitor specification, the size of the *Pixel-Planes* array, and the desired image size on the monitor. The 525 line (interlaced) SONY monitor will be driven at 30 Hz with 262 noninterlaced lines. This format will result in a scan

line time of 63.5 microseconds, of which 11.1 microseconds are required for horizontal retrace. To spread the 64 pixels across the entire screen and still use the internal 32 MHz oscillator requires a V clock period of approximately 750 nsec (64 x 750 nanoseconds = 48 microseconds - providing a display across 94% of the active area). The **SlowVHLXR**microcode bit should be used for display sizes of less than 128 pixels.

2.5.3.2 Functional Test

The system level description describes how the operator executes the test to determine active *Pixel-Planes* chips. This section describes the microcode necessary to set up the test.

For the functional test, the **SlowVHLXR** clock must be selected. The **TestVidWrL** signal for the video test memories is generated every **Px** clock cycle by the clock generation module. The **TestVidEnaL** microcode bit must be high to write a bit into the test memory. The **V** clock signal increments the test memory address counter. The **V** and **LBdEnaL** bits must be correctly manipulated by the microcode to enable the proper data to the memories. The **VTCnt⟨0:2⟩HEXF** bits can be used along with these signals to insure that only 2K data words are written into the memory. After the memory is full, the data is read out from the MULTIBUS interface, **VTCnt⟨0:2⟩HEXF** bits are manipulated to enable the next few scan lines of data, and the process is repeated until all desired data is unloaded from the memory. If not all bits are to be read on each scan line, the **V** clock signal must be modified appropriately.

2.5.3.3 Initialization

Once the host has determined which *Pixel-Planes* chips are active and which are not, (either by performing a functional test, or storing the data from previous testing) the *Pixel-Planes* chips must be initialized by loading the alive bits and the X-Y registers, followed by setup of the VC for scanout.

During the setup of the alive and X-Y registers, the **PxSel⟨0:1⟩HLXR** bits should select **CCLK*/4**, and the **MBMCEnaH**bit should be set.

2.5.3.3.1 Alive Register Load

The state of the alive bit on each *Pixel-Planes* chip indicates whether that particular chip is active or inactive. The host computer directs the VC to connect the scan path to the *Pixel-Planes* alive bits by setting scan control bit **ScCnt1HLXR** to 0 and **ScCnt0HLXR** to 1. The host computer transmits data words to the VC that contain the alive pattern. This data is shifted into the array least significant bit of each word first.

It should be noted that the VC is only capable of shifting data in 16 bit quantities. Therefore if the total number of bits to be input is not a multiple of 16, the extra bits required to make the total a multiple of 16 should be the *least* significant bits of the *first* word shifted into the array.

2.5.3.3.2 X-Y Address Configuration

The X and Y registers in each processing element must be initialized to the position of that pixel in the frame buffer. The host computer directs the VC to connect the scan path to the X-Y registers by setting scan control bit **ScCnt1HLXR** to 1 and **ScCnt0HLXR** to 0. The host computer transmits data words to the VC that contain the X-Y address patterns. This data is shifted into the array least significant bit of each word first. registers at each pixel. The data is sent X data followed by Y data, LSB first.

It should be noted that the VC is only capable of shifting data in 16 bit quantities. Therefore if the total number of bits to be input is not a multiple of 16, the extra bits required to make the total a multiple of 16 should be the *least* significant bits of the *first* word shifted into the array.

2.5.3.3.3 Video Controller Initialization

To load the microcode and color lookup tables, the **MBMCEnaH** bit must be set in the control register.

The memories are loaded by accessing the appropriate MULTIBUS address. The actual data to be loaded into the memories is described below.

After the memories are loaded, the proper control bits for display must be set up in the control register. The **Px** and **V** clocks must be set to the appropriate frequencies, the **MBMCEnaH** bit must be low, the **ScCnt⟨0:1⟩HLXR** bits must be high, and the **LoResEnL** bit must be low.

2.5.3.4 Horizontal Syncronization Microcode

The horizontal syncronization microcode RAM is 256 x 8 bits, and stores syncronization, blanking, and control signals for one horizontal line. For the prototype, the monitor will be driven at 30 Hz with 262 noninterlaced lines. This results in a horizontal line time of 63.5 microseconds, which is 254 **Px** clock cycles, so memory locations 0 through 253 are used. Ths **SlowVHLXR** clock will be used, and output once every three **Px** cycles, Each pixel will be displayed for 750 nanoseconds. The 64 pixels will not cover the entire screen, so the blanking perior is longer than the standard RS-170 blanking time. The sync signals are standard RS-170. A **V** clock signal must be generated every time the sync or blanking signal changes to that the data is latched into the hybrid output chip. The location in the microcode memory of the blanking and sync signals must be moved one location depending on whether or not the **SlowVHLXR** clock is selected due to different delays in the hardware. **Must add more details on this stuff later**

2.5.3.5 Vertical Control Microcode

Using 262 line noninterlaced display, the vertical control microcode RAM requires 524 locations (2 per line). The syncronization selection bits select standard RS-170 sync signal times. The vertical blanking signal is longer than the standard 20 lines because only 192 lines are used for active display (64 pixels x 3 lines per pixel). Locations 0-89 have vertical blanking set, and the **VTCnt⟨0:2⟩HEXF** bits set to disable. Location 90 and 91 select the even video train microcode, followed by 4 locations of normal microcode. Then a repeating pattern of 2 locations of pixel address increment microcode and 4 locations of microcode is stored until location 473. The screen is then blanked until location 522, where the end of field signal resets the counter, and the vertical sync signal is generated for the next frame. **add some more detail here**

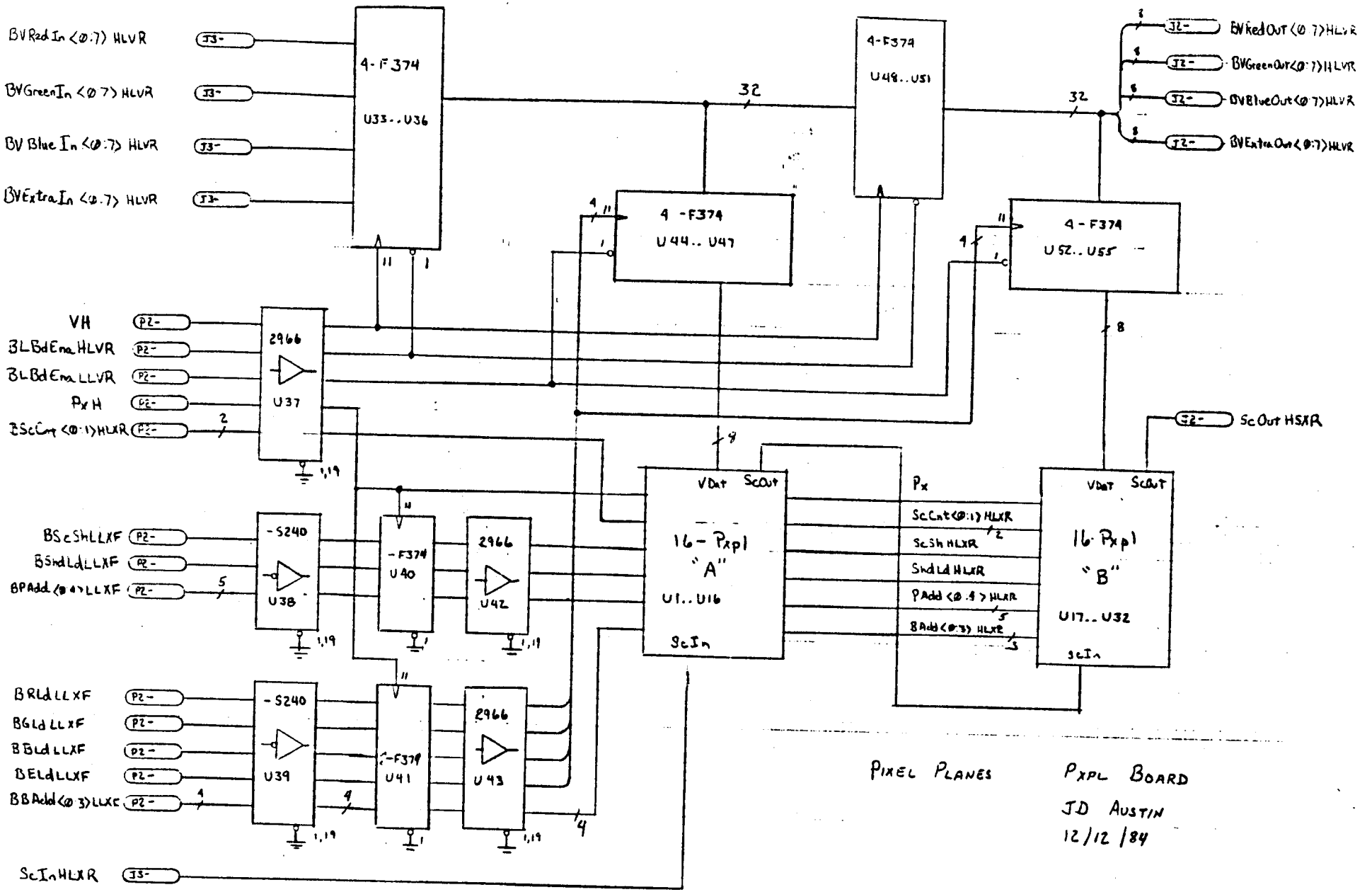
2.5.3.6 Video Train Microcode

must add a paragraph on the basic setup of the vertical mircocode. Include the timing diagram.

The disabled section has all signals set inactive. The even is identical to the normal section except the pixel address is set to zero instead of staying as it was on the previous line. The pixel address increment is the same as the normal except the pixel address is incremented at the beginning of the line.

2.5.3.7 Color Lookup Tables

The RGB color lookup tables in the Intech RGBDAC8T hybrid allow 256 locations of 8 bits for each of the red, green, and blue data. The **MBMCEnaH** bit must be set to access the memories. Normally the lookup tables will be loaded with the data equal to the address. For linearized displays, this data will be modified to produce linearized output for the monitor being used. The data in the lookup memories cannot be read from the MULTIBUS.



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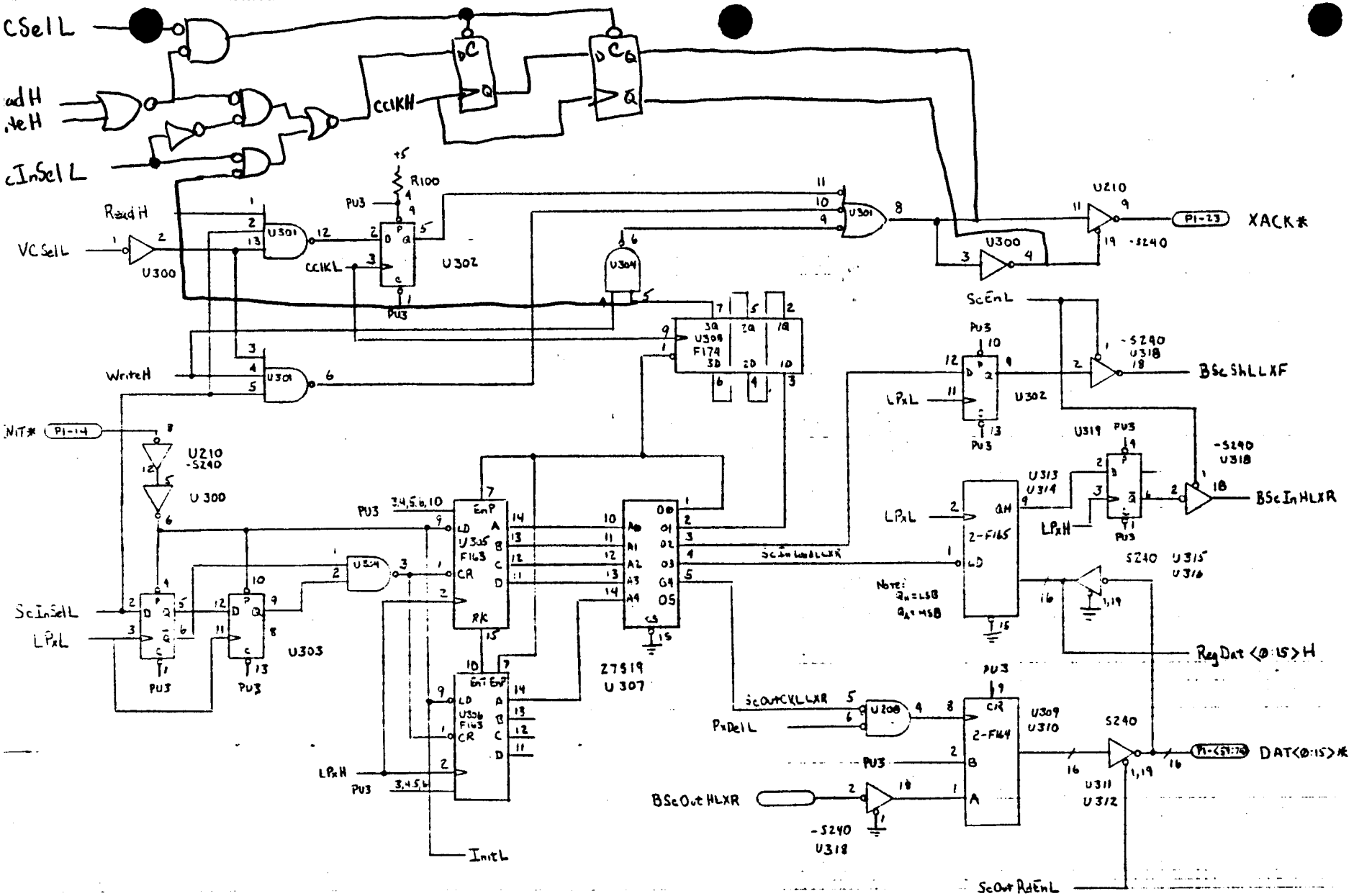

SPARES

U 300	F04	D, E, F
U 304	F00	C, D
U 319	F74	B

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VIDEO CONTROLLER

SCAN REGISTERS AND
XACK GENERATION
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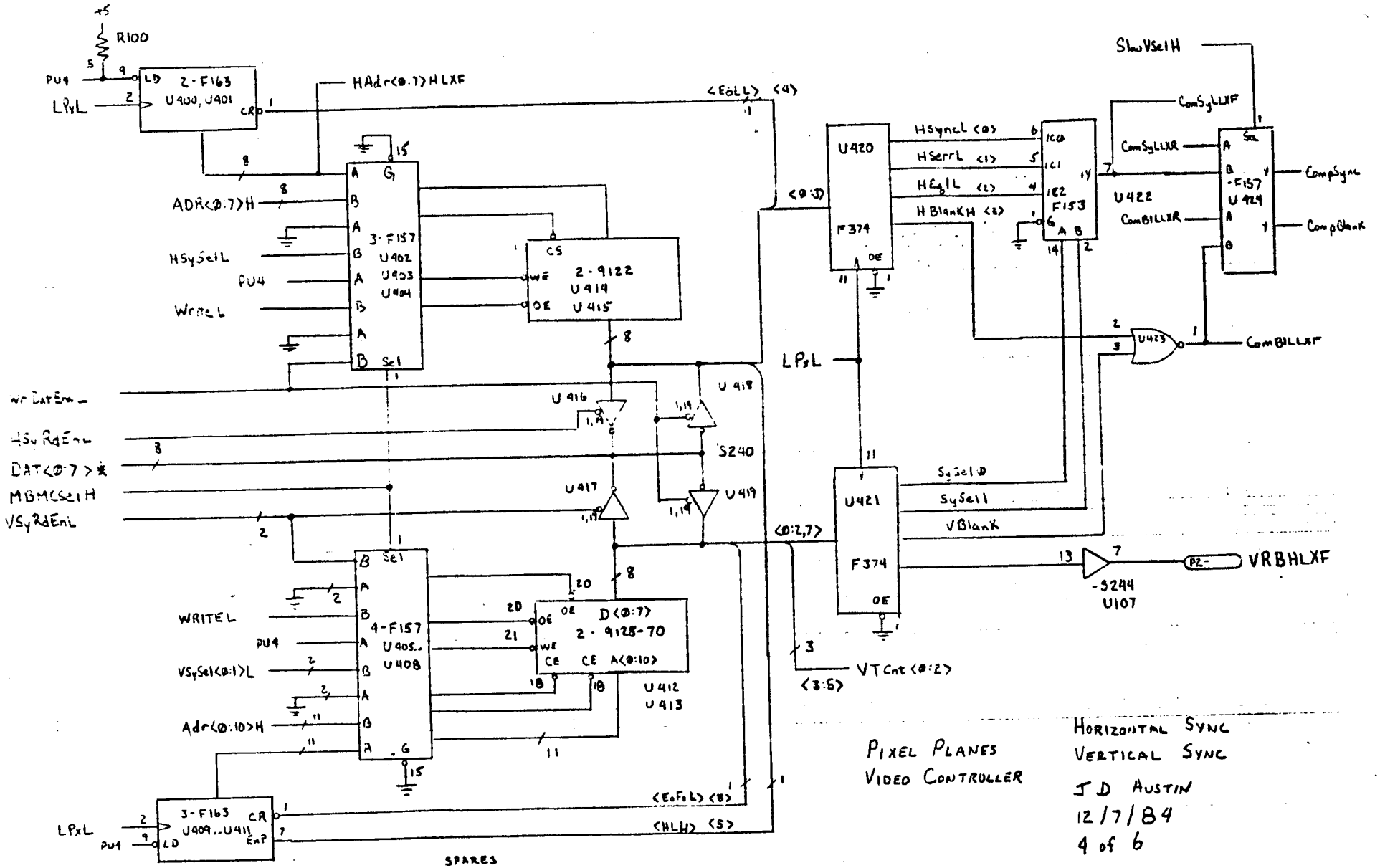
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R100
PU4
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LD 2-F163
U400, U401
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U420
F374
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HSerrL <1>
HEqlL <2>
HBlankH <3>
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U422
ComBLLR
ComSyLLR
ComSyLLXF
SlwVSelH
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U107
VTCnt <0:2>
<3:5>
4-F157
U405..
U408
WRITEL
PU4
VSySel<0:1>L
Adr<0:10>H
D<0:7>
2-9128-70
CE CE A<0:10>
U412
U413
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CR
ENP
LD
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SPARES
U423 FO2 B, C, D
Pixel Planes
Video Controller
Horizontal Sync
Vertical Sync
JD Austin
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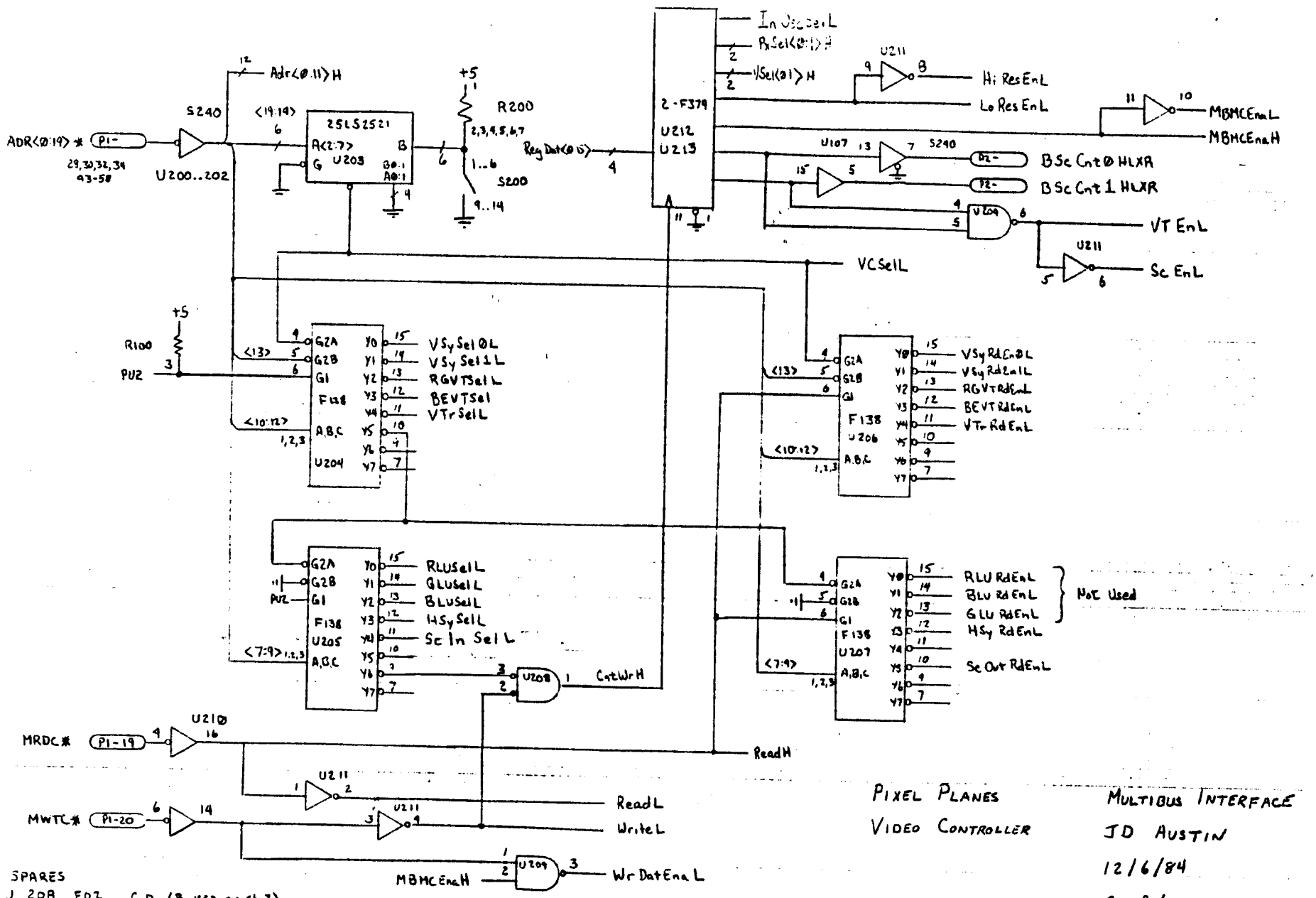

SPARES

- U208 F02 C,D (B USED ON SH 3)
- U209 F00 C,D
- U211 F09 F

NOTE: U210 SPARES COMPLETELY USED ON SH 1 AND 3

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VIDEO CONTROLLER

MULTIBUS INTERFACE

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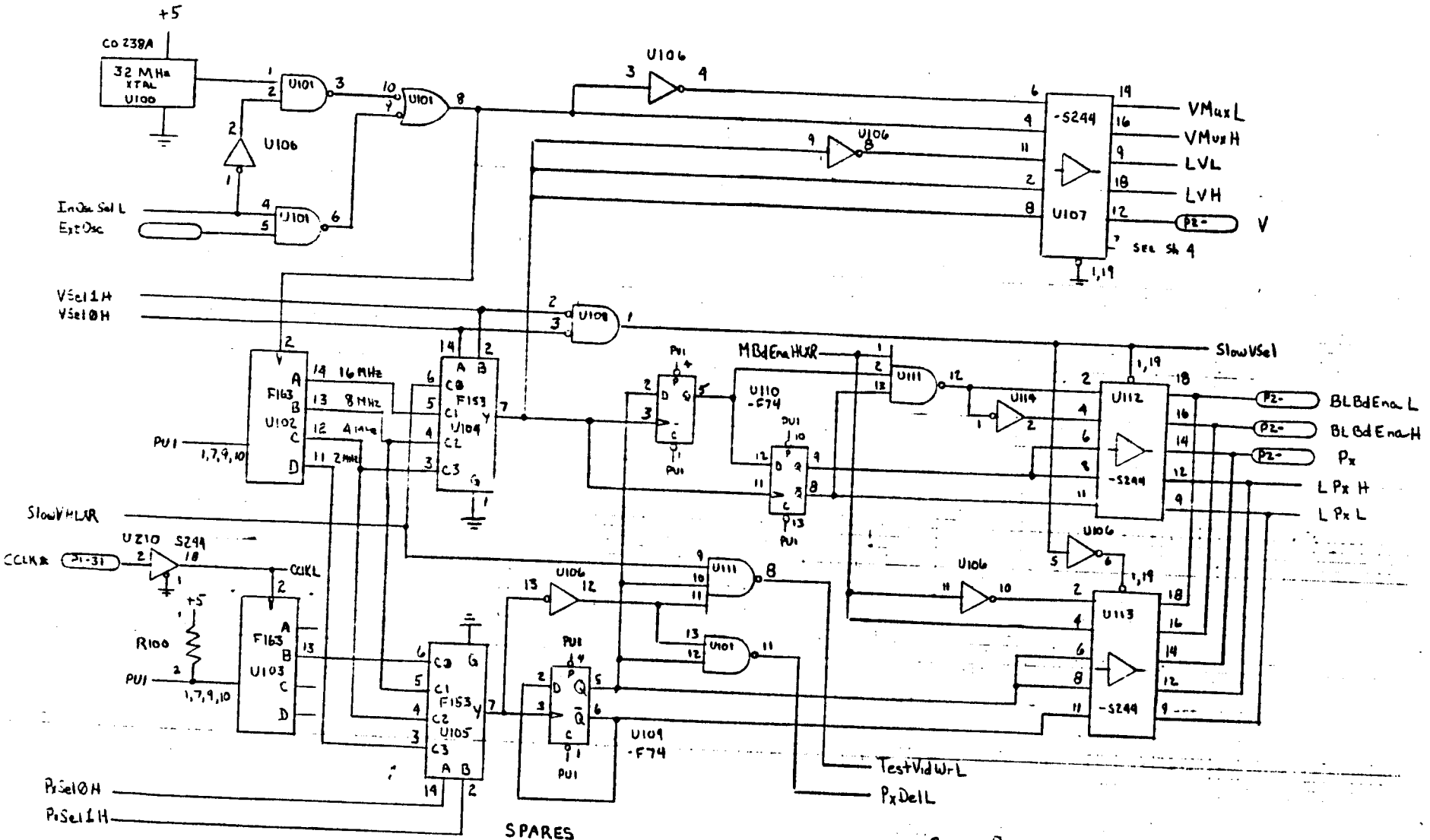

SPARES

U108	-F02	B, C, D
U109	-F74	B
U110	-F10	C
U107	-S244	G, H (F USED ON Sh 4)
U114	-F04	B, C, D, E, F

PIXEL PLANES
VIDEO CONTROLLER

CLOCK GENERATION
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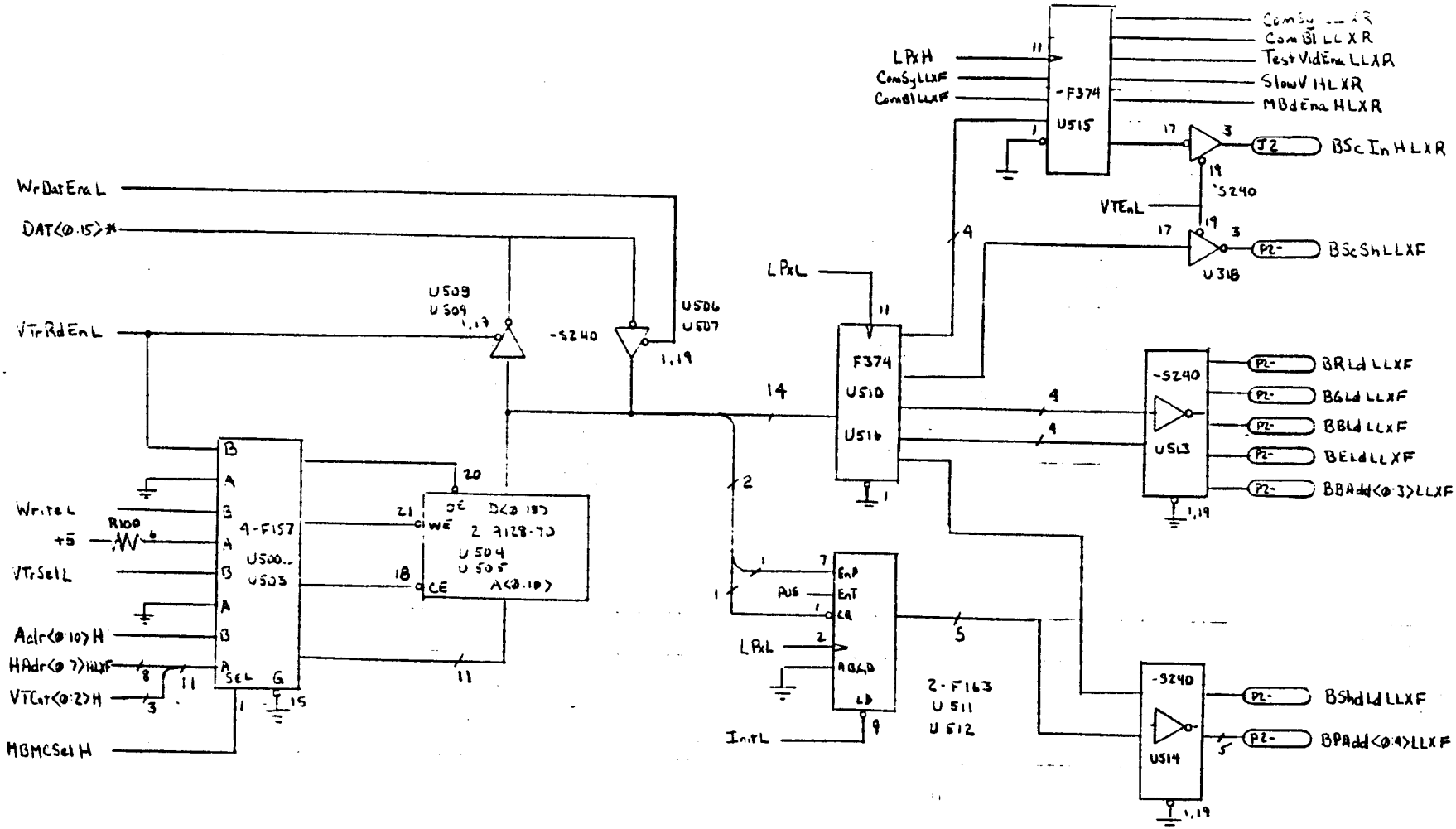

PIXEL PLANES

VIDEO CONTROLLER

PIXEL CONTROL

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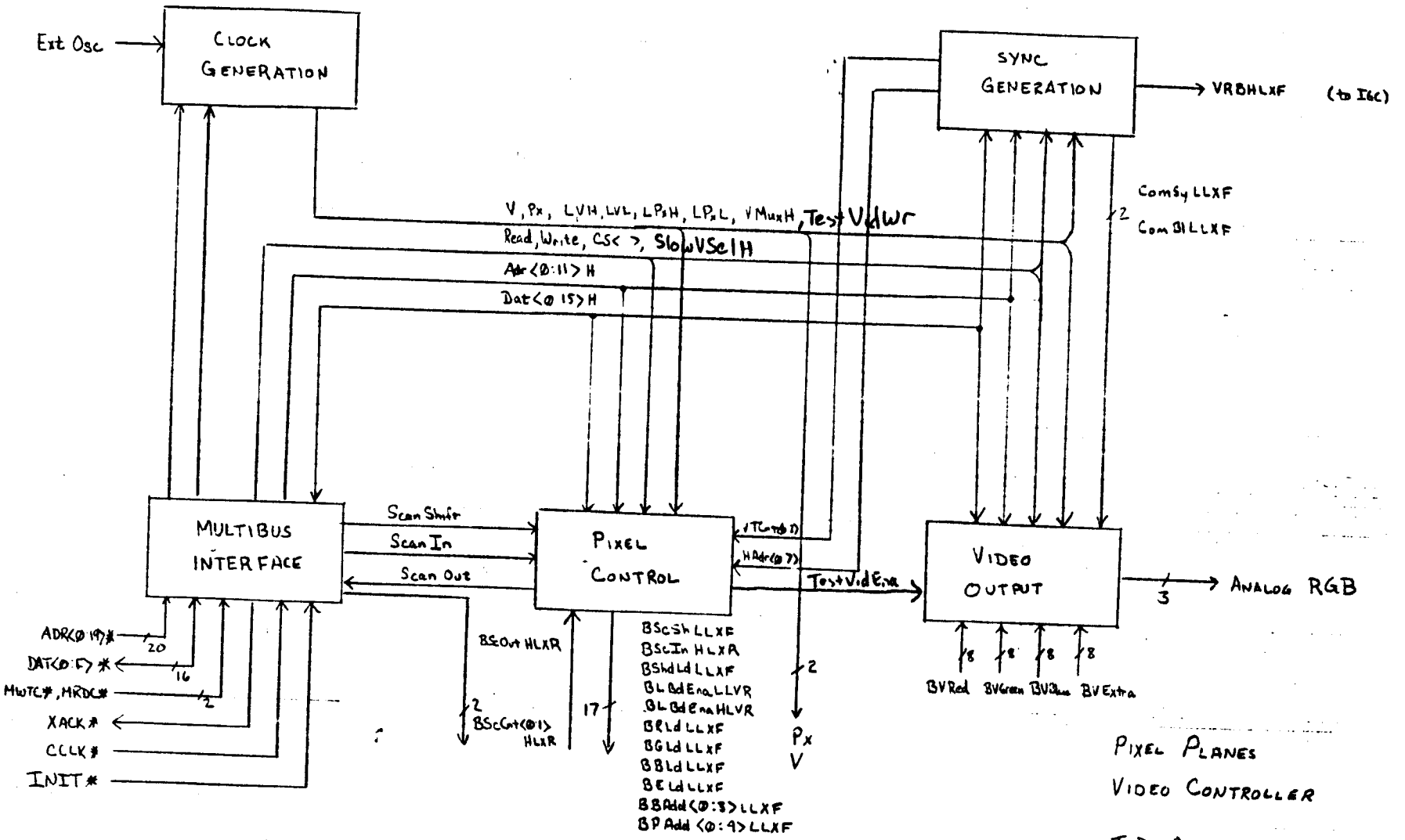
Ext Osc
CLOCK GENERATION
SYNC GENERATION
VRBHLXF
(to I6C)
ComSyLLXF
ComBlLLXF
V, Px, LVH, LVL, LPxH, LPxL, VMuxH, TestVidWr
Read, Write, CS< >, SlowVSclH
Adr<0:11>H
Dat<0:15>H
MULTIBUS INTERFACE
Scan Shift
Scan In
Scan Out
PIXEL CONTROL
VIDEO OUTPUT
Test+VidEna
ANALOG RGB
ADR<0:19>*
DAT<0:F>*
MWTC*, MRDC*
XACK*
CCLK*
INIT*
BScOut HLXR
BScCnt<0:1> HLXR
BScSh LLXF
BScIn HLXR
BShdLd LLXF
BLBdEna LLVR
BLBdEna HLVR
BRLd LLXF
BGLd LLXF
BBLd LLXF
BELd LLXF
BBAdd<0:3>LLXF
BPAdd<0:9>LLXF
Px
V
BVRed
BVGreen
BVBlue
BVExtra
Pixel Planes
Video Controller
J. D. Austin
12/13/84