HAL RVD-1002 VISUAL DISPLAY SYSTEM

INSTRUCTION MANUAL

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QUALITY COMMUNICATIONS EQUIPMENT

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WARRANTY

The HAL Communications RVD-1002 Visual Display System is fully guaranteed against defects in materials and workmanship for a period of one year. Should repair or replacement parts be required, notify HAL Communications Corp. promptly. The warranty period is measured from the date of the original invoice to the postmark date of your notification letter. Please do not return your unit to the factory for repair or adjustment until you have received a written return authorization.

HAL Communications assumes no responsibility for the repair or replacement of parts for units which have been damaged, abused, improperly installed, or modified and reserves the right to change the design of this visual display system without incurring obligation to incorporate such changes into existing units.

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ILLUSTRATIONS

1. INTRODUCTION AND SPECIFICATIONS

The HAL Communications RVD-1002 is a visual display system capable of decoding, storing, and displaying up to 1000 alphanumeric characters on the screen of a video monitor or television receiver.[1] When used with a suitable demodulator (terminal unit), it provides instant, silent reception of radioteletype signals.

Display Characteristics

The 1000-character display "page" is divided into 20 lines of 50 characters each. Characters are produced by a pattern of bright dots on a dark field. The matrix of 35 dots used to display each character is arranged in five vertical columns of seven dots apiece, as shown in Figure 1.1. The character height is equal to the space required for seven horizontal scan lines. The width is five sevenths of the height. The actual size of the displayed characters depends, of course, on the size of the monitor screen. Complete display specifications are given in Table 1.1.

The first incoming characters appear on the bottom line of the display. When that line is full, all characters in it shift up one line, leaving the bottom line blank and ready to receive new characters. This linefeed process recurs each time the bottom line becomes full, when a line feed character is received, or when the operator pushes the manual line feed button. When all 20 lines have been used, the next line feed causes the top line to be deleted.

Input and Output Characteristics

The display system accepts inputs in the form of serially transmitted, five-level, Baudot-coded characters, the standard for amateur radioteletype and many other types of data transmission. It operates at all standard input speeds (60, 66, 75, and 100 words per minute) and is compatible with the Mainline series of terminal units, as well as with any terminal unit which provides a low-voltage serial output. Complete input specifications appear in Table 1.2.

Figure 1.2 shows the input data pulse format. The code for each character consists of a start pulse, five data pulses, and a stop pulse. Each pulse may represent either a "mark" or a "space." Space pulses are positive with respect to ground; mark pulses are negative. The first pulse for any character is a space. Data pulses 0 through 4 follow the initial space and may be either marks or spaces, depending on the character being received. The stop pulse is a mark.

All of these "select" pulses are of equal length except the stop pulse, which may be longer. The select pulse length varies with the operating speed, as indicated in Table 1.2.

The input voltage must fall between +5V and +15V for space pulses, and between -5V and -15V for mark pulses, as shown in Figure 1.3. Pulse voltages falling in the forbidden region between -5V and +5V will cause display errors. The input voltage, however, can be made compatible with TTL logic levels, as explained in note 1 of Table 1.2. An optional loop interface allows the RVD-1002 to be connected directly in a DC machine loop if desired. See Table 1.2.

Operating Temperature

Performance of the RVD-1002 is guaranteed for ambient temperatures from 65° F to 80° F. However, the system will generally operate properly at temperatures from 50° F to 95° F. Convection cooling is provided by perforations in the top and bottom covers.

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[1] The video monitor is not supplied with the RVD-1002. An optional monitor is available. Section 5 provides instructions for modifying a television receiver to serve as a monitor.

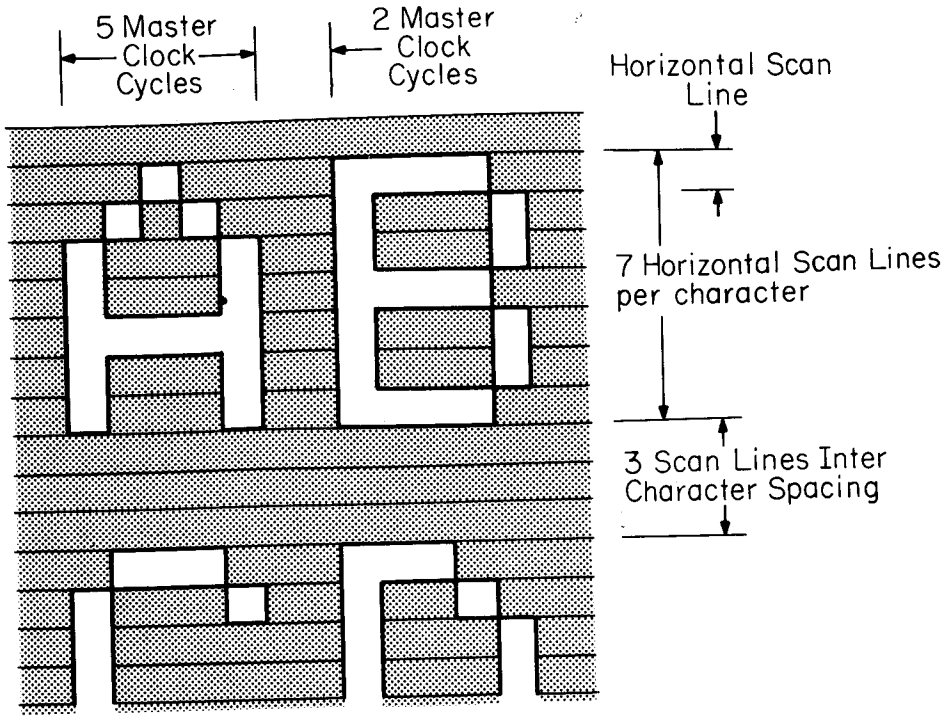


Figure 1.1 Character Display Format

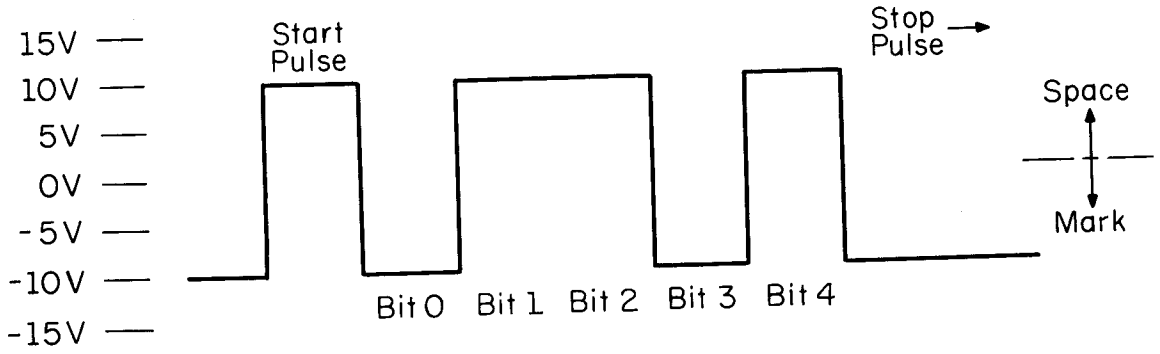


Figure 1.2 Input Word Format

Construction and Physical Specifications

The system is constructed on five three-by-six inch plug-in printed circuit cards, housed in an attractive two-tone grey cabinet. A rack-mounting model, the RVD-1002R, is also available. It is electrically identical to the standard model.

Size:	RVD-1002 3½" H, 17" W, 12" D RVD-1002R 3½" H, 19" W, 12" D
Weight:	10 pounds (approx.)
Shipping Weight:	15 pounds (approx.)
Overseas Shipping Weight:	17 pounds (approx.)

Accessories

The RVD-1002 is supplied complete with a standard ¼" phone plug and three feet of two-conductor shielded wire for constructing the required input cable.

TABLE 1.1: DISPLAY SPECIFICATIONS

Character format	5 x 7 dot matrix
Line format	50 characters/line
Page format	20 lines/page
Character width-to-space ratio	5:2
Character-plus-space time[1]	875 nanoseconds
Line height-to-space ratio	7:3
Horizontal scan lines per character line	7
Horizontal scan lines per intercharacter space	3
Horizontal line display percent[2]	70%
Vertical field display percent[3]	76%

[1] Defined as the time required during a horizontal scan to display one character plus an intercharacter space.

[2] Defined as the percentage of the horizontal line used in displaying 50 characters and the spaces between them.

[3] Defined as the percentage of the vertical field used in displaying 20 character lines and the interline spaces.

TABLE 1.2: INPUT SPECIFICATIONS

Input data form	Serial
Word format	
Pulse 1	Start pulse
Pulse 2	Data pulse 0
Pulse 3	Data pulse 1
Pulse 4	Data pulse 2
Pulse 5	Data pulse 3
Pulse 6	Data pulse 4
Pulse 7	Stop pulse

TABLE 1.2: INPUT SPECIFICATIONS (Cont.)

Select pulse length	
60 WPM	22 milliseconds
66 WPM	20 milliseconds
75 WPM	17.57 milliseconds
100 WPM	13.47 milliseconds
Start pulse length	Same as select pulse
Data pulse length	Same as select pulse
Stop pulse length	Greater than or equal to select pulse
Start pulse state	Space
Stop pulse state	Mark
Mark Voltage[1]	−5 V to −15 V
Space Voltage	+5 V to +15 V
Input impedance	500 ohms or greater
Loop interface option	
Input mode	Current Sensing
Input current range	
Mark	20-100 ma.
Space	0-1 ma.
Input impedance	10 megaohms or greater

[1] The input can be made compatible with TTL logic by removing the 470-ohm input resistor on circuit board SC-B4 and replacing it with a jumper. In that case the mark voltage range is from 0 to +0.8 V and the space voltage range is from +2.4 to +5.0 V.

TABLE 1.3: VIDEO SPECIFICATIONS

Lines per field	262.5
Fields per frame	2
Lines per frame	525
Line rate	15.750 kHz
Field rate[1]	60 Hz
Timing tolerance	±0.1%
Synchronization voltage	0.35V peak-to-peak
Synchronization polarity	negative
Video voltage[3]	0.60 V peak-to-peak
Composite video signal voltage	1.0 V peak-to-peak
Voltage tolerance	±10% with specified load
Peak video bandwidth[2]	4.0 MHz
Load impedance	75 ohms ± 5%

[1] Fields are automatically interlaced.

[2] Defined as the frequency above which all energy could be eliminated with no degradation of picture quality. Readability decreases noticeably when energy below 3.4 MHz is eliminated.

[3] Figure 1.4 shows the proper video output waveform.

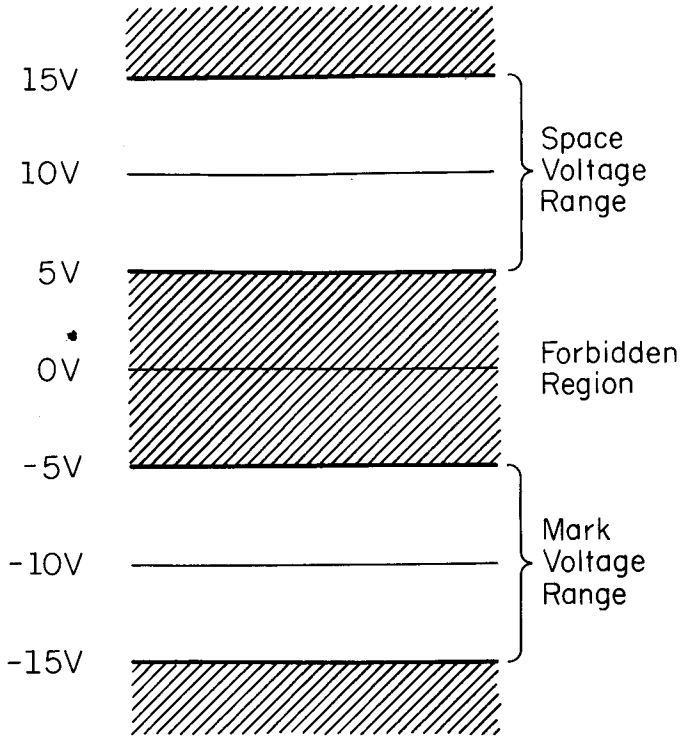


Figure 1.3 Input Voltage Limits

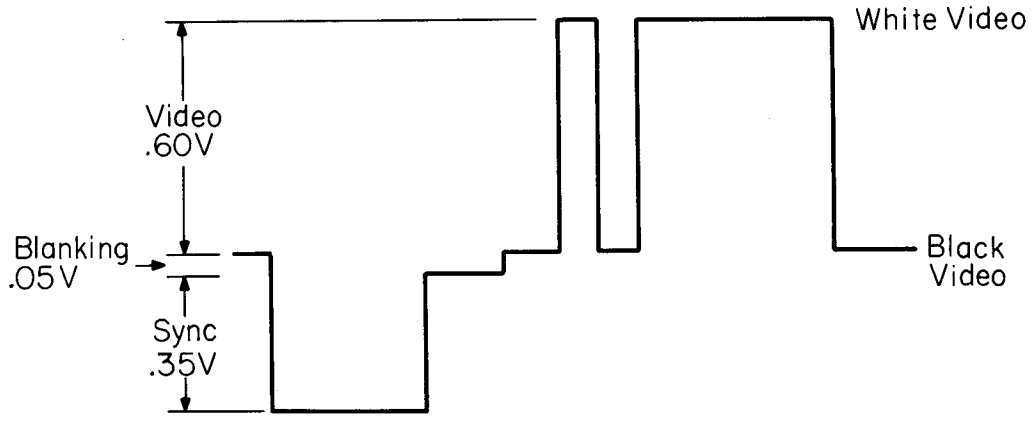


Figure 1.4 Video Output Format

2. INSTALLATION AND OPERATING INSTRUCTIONS

Installation

The RVD-1002 is very simple to install, as Figure 2.1 illustrates. First, connect the output of the terminal unit (TU) to the serial input jack, using the phone plug and shielded cable supplied with your unit. If you are using a terminal unit other than the Mainline series, be sure that the output voltages meet the requirements shown in Figure 1.3.

Use 75-ohm coaxial cable (such as type RG-59/U) to carry the video output of the RVD-1002 to the video monitor. The output jack mates with a type BNC plug.

NOTE: The video output line must be terminated by a 75-ohm impedance. Check the monitor specifications to determine whether its input represents a 75-ohm load. The load need not provide a DC return path.

Connect the AC cord to a source of 115 volt 60 Herz power. *Connect the RVD-1002 only to a three-wire grounding AC system* to protect the operator from electrical shock and to minimize interference from stray RF fields.

When mounting your unit, check that the ventilation holes in the top and bottom covers are not obstructed. Avoid mounting it above units which generate heat.

You may easily modify a standard television set for use as a video monitor. Full details are given in Section 5 of this manual. *DO NOT,* however, use a television set in which one side of the AC power line is connected directly to the chassis or to the ground return for the circuitry unless you supply AC power to the set from a reliable isolation transformer.

Operation

The RVD-1002 is as simple to operate as to install. The eight-section pushbutton switch on the front panel controls all functions. The switch is shown in Figure 2.2.

AC POWER SWITCH AND SPEED SELECTORS — The OFF button, furthest to the right, is the power switch. When it is depressed, power to the unit is turned off. The four buttons to the left of the power switch select the operating speed of the system. To switch the unit on, press the button corresponding to the speed (in words per minute) of the incoming signal. The speed may be changed at any time without turning the power off by simply depressing one of the other speed selector switches.

UNSHIFT ON SPACE — The button to the left of the four speed selectors activates the automatic "letters-shift" circuitry, causing the display to return to letters case every time a space character is received. This feature prevents the monitor from erroneously displaying numbers instead of letters if a letters shift character is not received at the proper time.

MANUAL LTRS — Pushing the momentary-contact manual letters button inserts a letters-shift character into the input circuitry, causing the system to shift from numbers to letters case. The letters-shift character will override the input case control characters being received while the button is depressed.

MANUAL LF — The manual linefeed control is also a momentary action switch. Pushing it generates a linefeed character which overrides the incoming signal and causes all characters on the screen to move up one line. Whenever a linefeed character occurs, whether it is received at the input or generated by pushing the manual linefeed button, a carriage return command is automatically produced. The next character received is therefore displayed at the left margin.

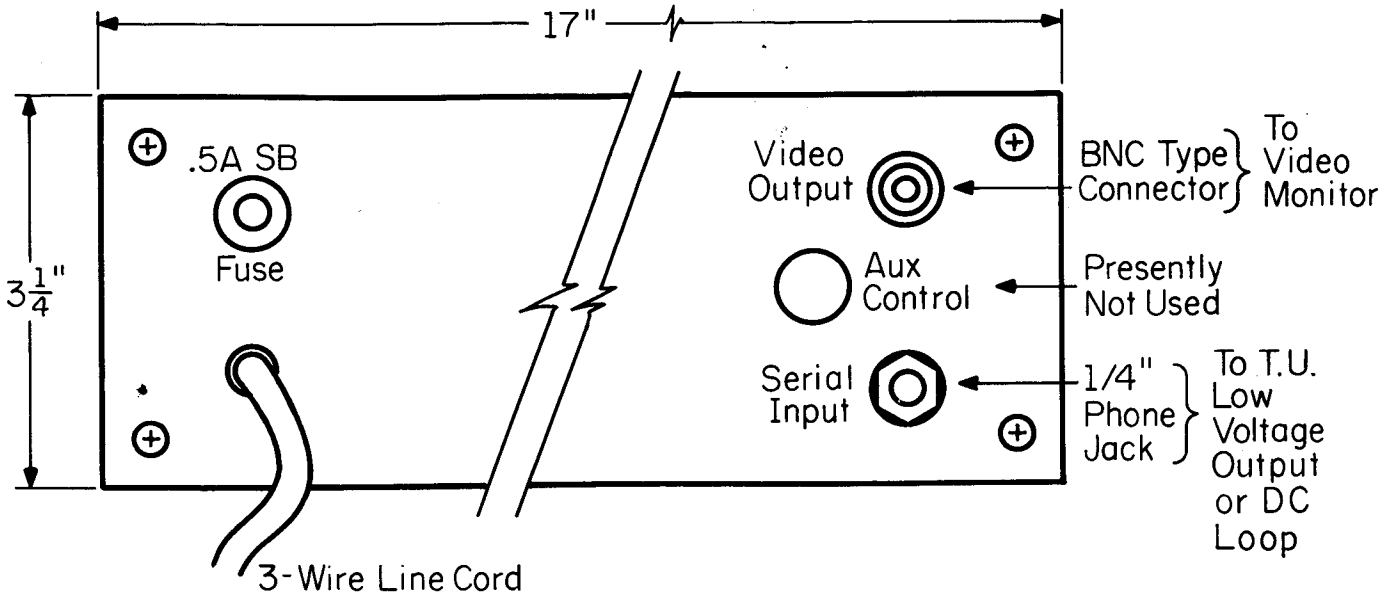


Figure 2.1a Rear Panel Connections

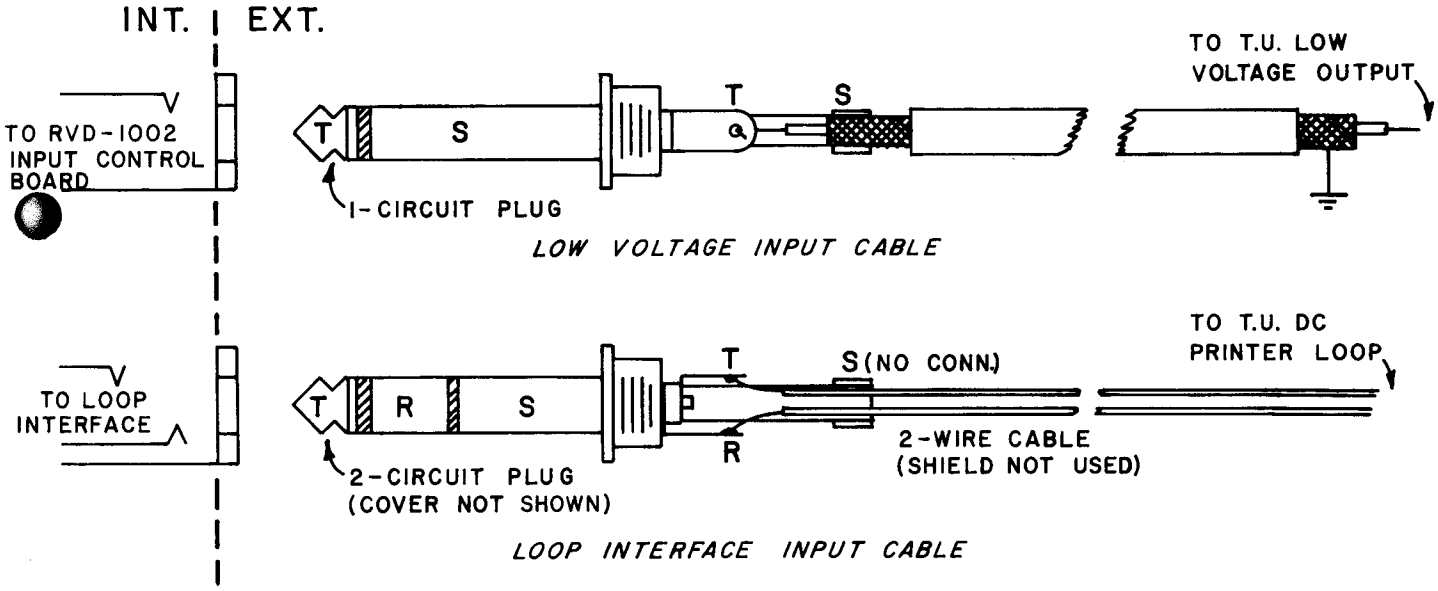


Figure 2.1b Input Cables

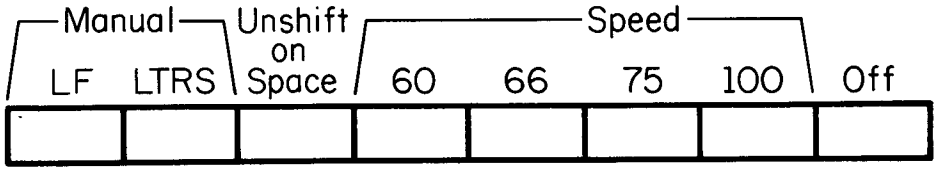


Figure 2.2. Front Panel Controls

3. THEORY OF OPERATION

Basic Operating Principles

The RVD-1002 circuitry is made up of two main subsections: (1) the input circuits, and (2) the memory and display circuits. The input section accepts each teletype character in sequence from the local loop or terminal unit, converts it from serial to parallel form, checks it to determine whether it is a printing character or a control code (such as a linefeed or carriage return), and stores it momentarily until the main memory is ready to accept it.

The memory and display section stores the incoming characters and maintains the display by continuously reading out the memory contents, generating the dot pattern required for each character and producing the composite video signal fed to the monitor.

Teletype Code

In the standard Baudot code used in five-level teletype work, each character is made up of seven sequential "select" pulses, as shown in the top trace of Figure 3.1. Pulses may have either of two states; in the "mark" state current flows in the printer loop, while in the space state it does not. The rest condition, when no characters are being transmitted, is always a mark.

In any character the first pulse, called the start pulse, is a space; it prepares the printer to accept the six succeeding pulses of that character. The five pulses which follow define the individual character. There is a unique pattern of these pulses for each character. The last pulse, called the stop pulse, is always a mark. It allows the printer to recover and prepare for the next character. All pulses are of equal length except for the stop pulse, which may be longer. The pulse length decreases with increased operating speed, as indicated by Table 1.2.

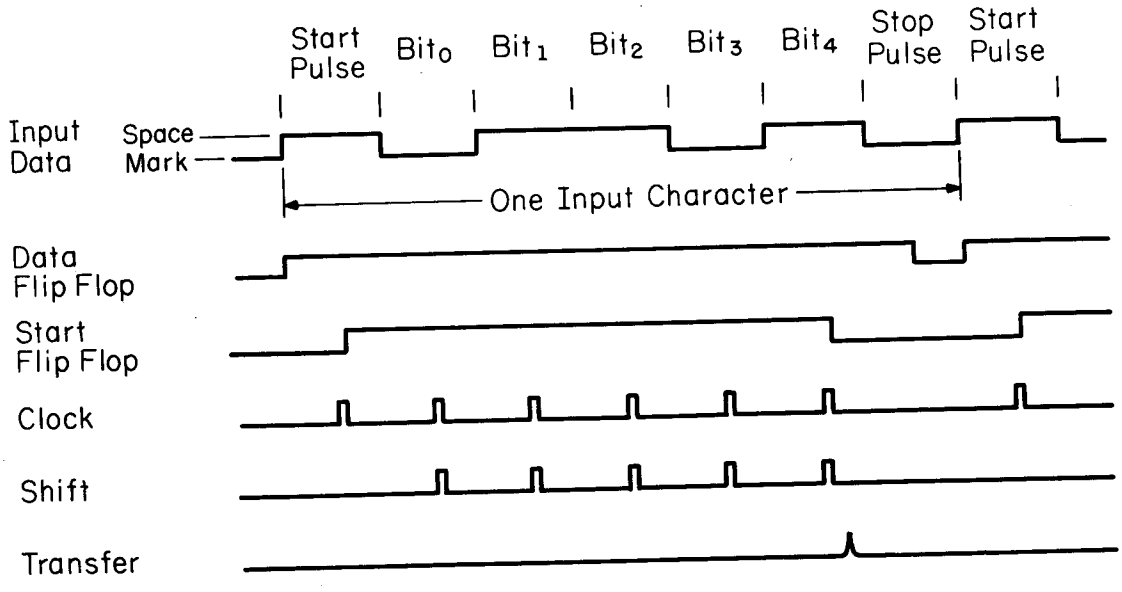


Figure 3.1 Input Timing

INPUT SECTION

The input section accepts the incoming teletype pulses for each character, "skims off" the start and stop pulses, and reads the remaining five pulses (the ones that define the character) into a shift register. The pulses, which have been received sequentially (in serial form), are then all available simultaneously from the outputs of the shift register's five stages. That is, they have been converted to parallel form and are ready for transfer to the page memory in the memory and display section.

The input circuitry operates independently from the memory and display section, interacting with it only when a character has been converted and is ready to be transferred. The input section is composed of these subcircuits:

1. Input oscillator
2. Start-bit detector and data sampler
3. Start flip-flop and bit counter
4. Data input shift register
5. Control code detector

A block diagram of the input section is given in Figure 3.2.

Oscillator

The operation of the input circuitry is synchronized with the speed of the incoming teletype signal by an internal oscillator, which runs at a frequency 2^{17} times the baud rate of the operating speed chosen. The required frequency stability is quite easily achieved with a crystal-controlled integrated-circuit oscillator.

The oscillator frequency and hence the system operating speed is selected by switching in one of four crystals. The speeds and their corresponding frequencies are given in the following table:

TABLE 3.1: INPUT OSCILLATOR FREQUENCY

Speed (WPM)	Baud Rate	Select Pulse Length (ms)	Oscillator Freq. MHz ± .1%
60	45.45	22	5.9578
66	50	20	6.5536
75	56.9	17.57	7.4599
100	73.7	13.47	9.7306

Start-Bit Detection

The first function of the input section is to check the incoming signal for a start pulse. The signal is fed directly to the DATA flip-flop. The leading edge of the first space pulse (the start pulse) sets this flip-flop, starting the oscillator and triggering a delay circuit, as illustrated in Figure 3.2. At the end of the delay period, which is about 7/16ths the duration of a select pulse, the incoming signal is sampled. If the space condition no longer exists, the pulse is considered a transient and the DATA flip-flop is reset. If, however, the space signal is still present at the end of the delay interval, the pulse is considered a valid start pulse and the START flip-flop is set.

Serial-to-Parallel Conversion

After the START flip-flop is set, the succeeding five data pulses are sampled and entered in a five-bit shift register. Since this data register is clocked by the oscillator delay circuit, each incoming

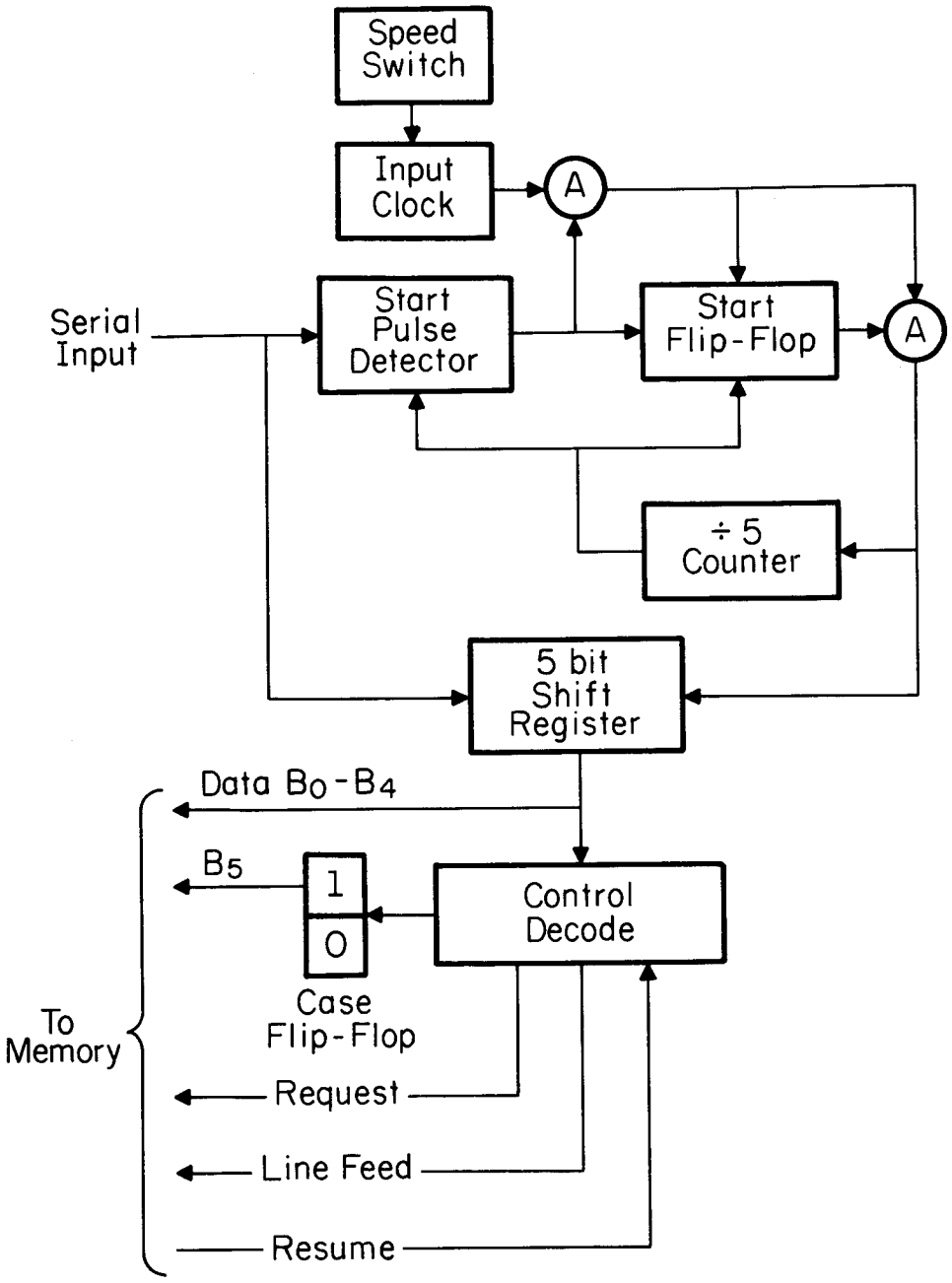


Figure 3.2 Input Section Block Diagram

pulse is sampled a little before the middle of its total duration, assuring that bias distortion in the input signal and transients near the beginning and end of the pulse do not cause errors.

The clock pulses are also fed to a bit counter, which keeps track of the number of data pulses read in. When the bit counter has been incremented five times, all five significant data pulses have been entered. The bit counter then clears the START and DATA flip-flops so that they are ready for the next incoming character. The five data pulses, which are now available in parallel format, are transferred into a buffer where they are held until the memory and display section is ready to receive them.

Control Code Checking

Control codes do not print on the screen, so they need not be entered in the page memory. They are detected and treated separately. A decoding circuit recognizes these five special codes (line-feed, carriage return, letter shift, figures shift, and blank) and instructs the logic circuitry how to handle them.

The blank and carriage return codes are ignored, since blanks do not affect the display in any way and carriage returns are produced automatically after each line-feed by the memory control circuits. If the control code is a line-feed, the input section transmits a signal directly to the memory and display section, causing a line-feed to occur at the end of the next memory cycle. The exact process will be described later.

A shift character affects those printing characters which follow it so this code is detected and used to either set or reset the CASE CONTROL flip-flop (depending on whether it is a letters-shift or figures-shift code). The output of this flip-flop enters the memory as a sixth data bit in parallel with the five pulses or "bits" for each printing character. When the memory is read out to produce the display, this sixth bit instructs the display circuitry which case to print.

Data Transfer

Once the incoming data has been stored in the data register and checked for control codes, it is ready for transfer to the memory and display section. If the stored data pulses do not represent a control code, a transfer pulse is generated, setting the ENTER REQUEST flip-flop. Its output, fed to the page memory control circuitry, indicates that a character has been assembled and is ready for transfer. At the appropriate instant in the memory cycle, the five data bits from the buffer register and the one bit from the CASE CONTROL flip-flop are fed in parallel to the memory. After the transfer is complete, the data entry circuit issues a "resume" command to the input circuit, allowing it to enter and convert the next character. The page memory cycle time is very short, so the entire transfer process can be completed during the stop pulse, which is not entered in the memory.

MEMORY AND DISPLAY SECTION

The memory and display section stores the character codes supplied by the input section, converts each one to a pattern of dots to form the display, and generates a composite video signal to drive the monitor.

The system incorporates three different memories. The first is the page memory, into which the incoming characters are written. Each time a row of characters is to be displayed, fifty characters are transferred from the page memory to the line memory, where they are stored temporarily and supplied, one at a time, to the character generator. A read-only memory in the character generator converts the teletype codes to the pattern of dots needed for the display.

The remainder of the memory and display section consists of the master oscillator, the video generator, and various control circuits. A block diagram is shown in Figure 3.3.

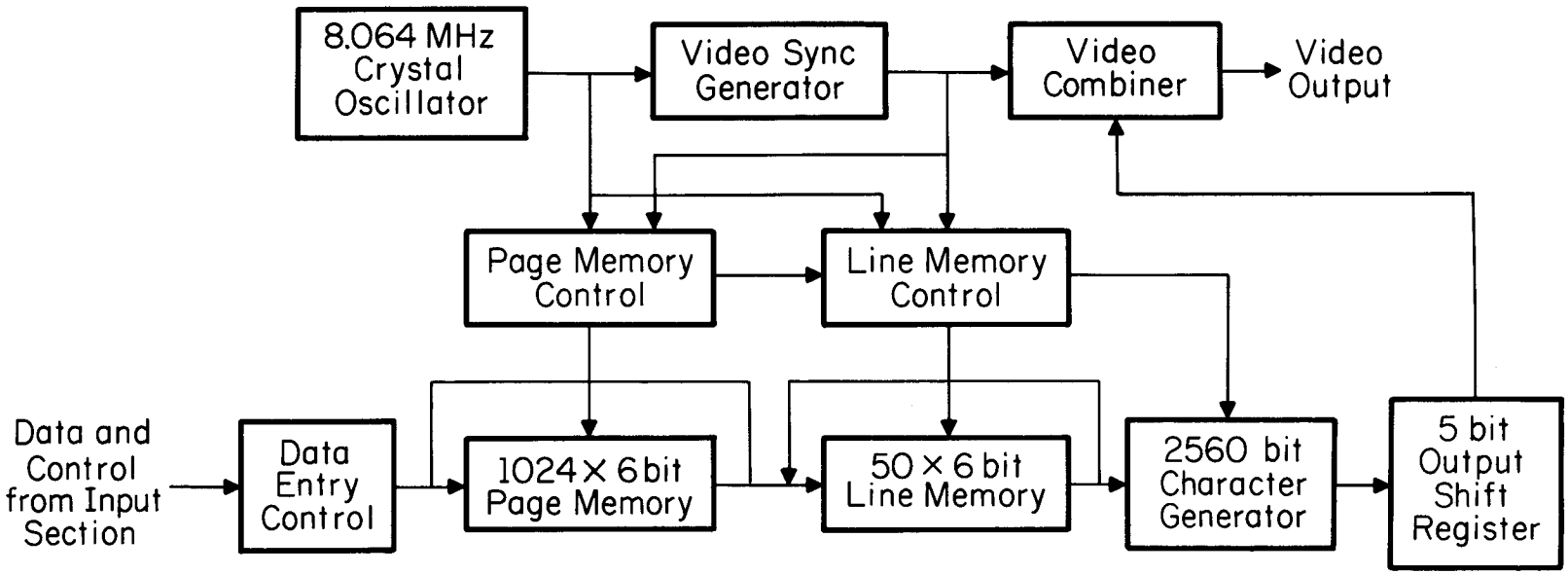


Figure 3.3 Memory and Display Section Block Diagram

Master Oscillator

All functions of the visual display system are accurately timed and synchronized by the crystal-controlled master oscillator shown in Figure 3.4. It is stable to within ±.1% of its 8.064 MHz operating frequency.

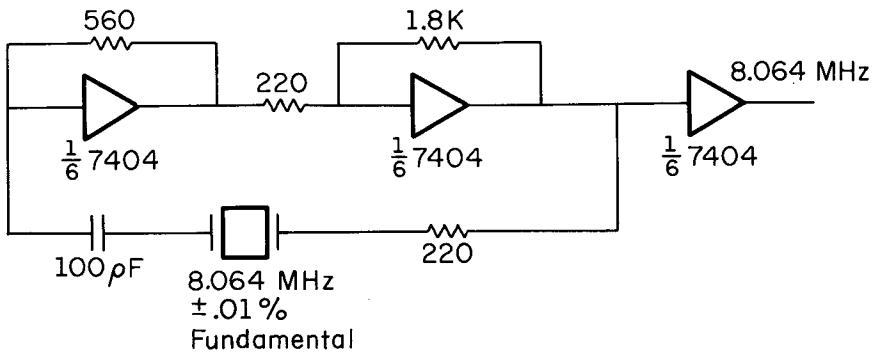


Figure 3.4 Master Oscillator Circuit

Page Memory and Control

The page memory stores all 1000 characters which make up a display "page" (20 lines of 50 characters each). Character codes in parallel format arriving from the input section enter the page memory; they are transferred in groups of 50 to the line memory where they are used to generate one horizontal row of characters in the display.

The page memory consists of six 1024-bit shift registers operating in parallel, as shown in Figure 3.5. Since only 1000 characters are stored at any time, the extra 24 locations in each register are unused. The first five registers store the five select pulses for each character; the sixth stores the output of the CASE CONTROL flip-flop. When characters are converted to dot codes, this sixth bit informs the character generator whether the accompanying five pulses represent a character in figures or in letters case.

The display, which conforms to U.S. television standards, is recreated or "refreshed" 60 times per second. That is, 60 complete video fields per second are interlaced to produce 30 complete video frames. The contents of the page memory are read out each time a new field is produced, once every 60th of a second.

To read out the memory, the shift registers are clocked by pulses derived from the master oscillator. The six bits for each successive character appear in parallel at the register outputs every time a clock pulse occurs. The readout process, however, must be non-destructive--the characters must be retained in the memory for use during succeeding video fields. As Figure 3.5 shows, feedback paths are provided between the output and the input of each register. At the same time that a character is read out to the line memory it is fed back to the page memory inputs (unless it belongs to a row which is to be deleted).

Although the memory contains 1,024 locations, only 1000 are used. The extra 24 locations which are not used must be accounted for during each complete cycle of the memory. Therefore, 24 extra clock pulses are supplied to the memory at the end of each video field during the vertical retrace interval. The memory cycle is then complete and the code for the first character is at the end of the memory registers, ready to be clocked out again when the next video field starts.

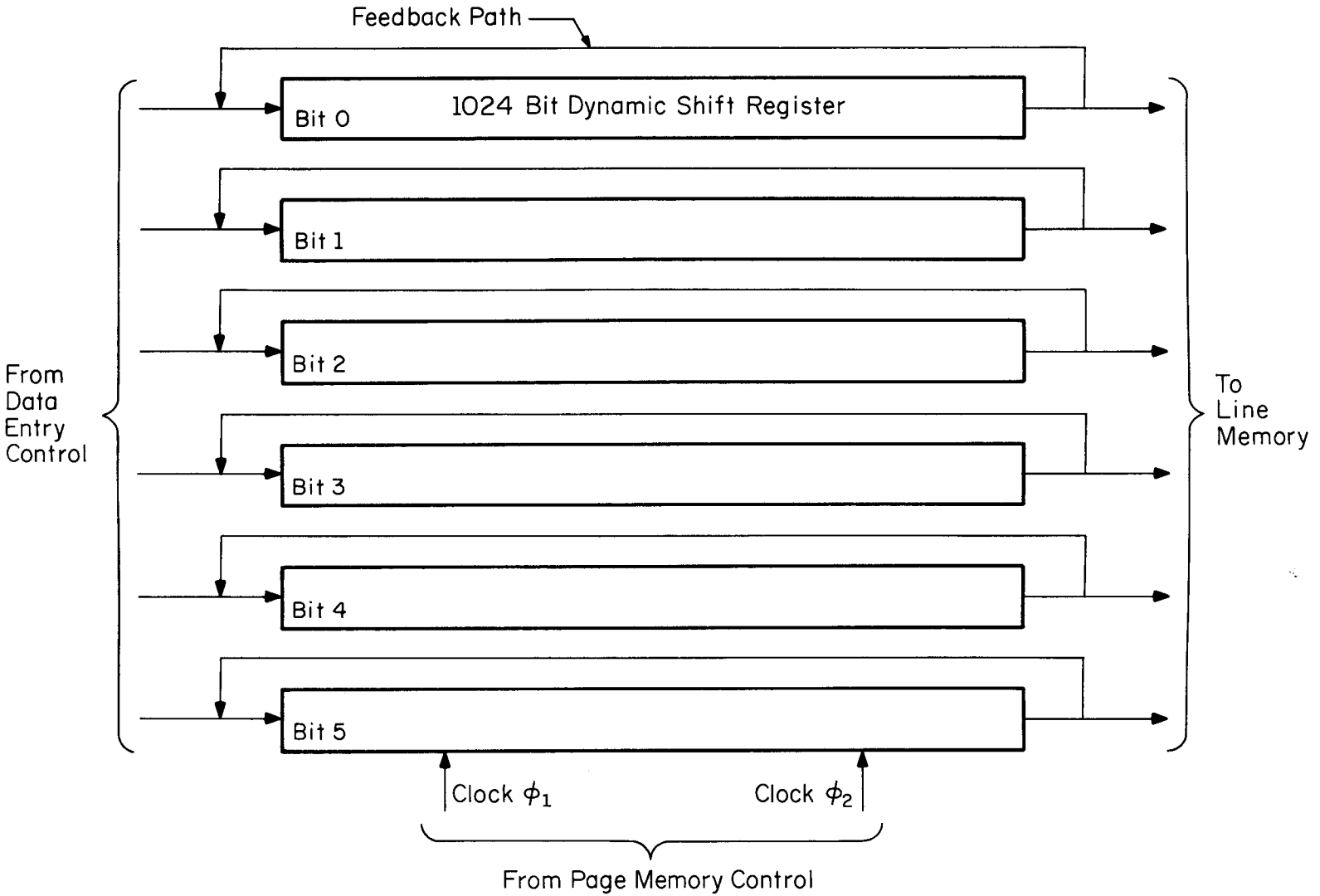


Figure 3.5 Page Memory Registers

The page memory control synchronizes the memory cycle with the production of each video field. When a row of characters is to be displayed, it passes 50 clock pulses to the page memory registers, causing 50 characters to be transferred to the line memory and also recycled to the page memory inputs. The memory is not clocked again until the complete row of characters has been produced, a process which requires ten video scan lines. Since there are 20 rows of characters per page, the clocking process is repeated 20 times for each video field.

At the end of a page, when all 20 rows have been displayed, an end-correction circuit generates the 24 extra clock pulses needed to complete the memory cycle. The horizontal sync pulse is fed to the shift register clock terminals and to a counter. When 24 pulses have been produced, the counter stops the clock pulses.

The page memory and its control circuits are located on circuit card SC-B3 and SC-B2.

Data Entry Control

Characters supplied from the input section must be transferred to the page memory at the correct moment in its cycle if they are to appear at the proper position on the screen. A character which has been assembled (converted from serial to parallel) in the input section is stored there momentarily until the page memory is ready to accept it. The data entry control synchronizes the transfer of the character to the page memory.

Three counters are used in the data entry section. As the page memory cycles, the stored-character counter keeps track of the number of characters read out; it cycles from 0 through 49 once for each row of characters displayed. When a complete row has been transferred to the line memory, this counter reaches 49 and resets to zero, incrementing the line counter by one. This second counter therefore records the number of the lines (from 0 through 19) being read out.

An incoming-character counter keeps track of the number of characters entered from the input section. As with the stored-character counter, it cycles from 0 through 49. At that point in the memory cycle when the line counter indicates that the last line is being read out and when the stored-character counter reads the same as the incoming character counter, the new character is entered in the memory. New characters therefore always appear in the bottom line of the display.

New characters are read into the page memory by breaking the feedback paths of the memory shift registers when the two character counters coincide. The previously stored character is therefore not fed back to the register inputs on the next clock cycle. The new character is entered in its place. The feedback path is then reestablished before another clock pulse arrives.

To illustrate this process, let us assume that the screen is filled except for the last line, and that nine characters have already been written in that line. A new character is assembled in the input section and the ENTER REQUEST flip-flop is set. The incoming-character counter contains the number nine, indicating that nine characters have already been entered in the row and that the new one will be the tenth. When the character has been entered, the counter is advanced to 10.

As the page memory starts through its cycle, the stored-character and line counters increment. When the line counter reaches 19, indicating that the last line is being read out, and the stored-character counter reads nine, showing that the first nine characters in the last row have been read out, the feedback path is broken, the next stored character is deleted, and the new one is entered in its place. The feedback path is then reconnected, the memory continues through its cycle, and the input section is free to assemble another input character. The next new character will be entered in the same manner on a later memory cycle.

Linefeed Control

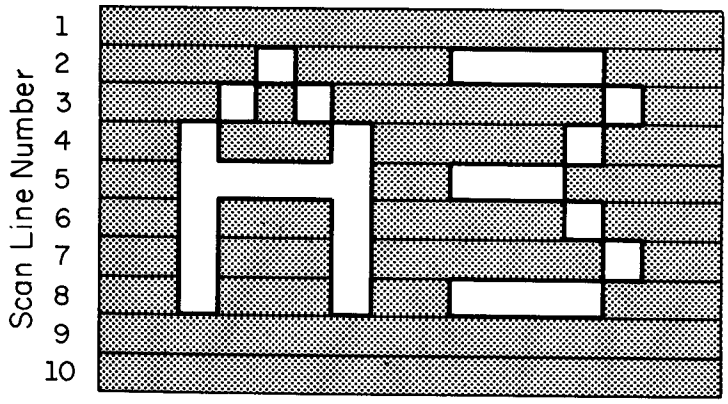
A linefeed command can originate from any of three sources: (1) the control code detector in the input section whenever a linefeed code is encountered, (2) the incoming-character counter when it reaches 49 and recycles to zero, indicating that the bottom line of the display is filled, and (3) the manual linefeed pushbutton. An output from any of these sources sets the LINEFEED flip-flop. When the various counters indicate that the last scan line of the character display is complete, the page memory feedback paths are broken and the memory is clocked an extra 50 times. The 50 characters which would otherwise have constituted the first row of the next display field are clocked out of the memory. Because the line memory is not active and ready to receive them, they are discarded. Space characters are supplied to the register inputs in their place so that the last line of the next display field will be blank. All other characters are moved up one line.

Whenever a linefeed occurs, the incoming-character counter is reset to zero. Consequently, the next new character is written at the leftmost position of the bottom line. In this way, a carriage return is automatically produced with each linefeed, regardless of how the linefeed command originated.

Line Memory and Control

Ten horizontal scan lines are used to display each row of characters, as Figure 3.6 illustrates. The first line is left dark. The next seven contain the dot patterns which make up the characters, and the remaining two are again left dark. The dark lines separate the rows of characters from each other. The line memory stores the characters while the ten lines are being scanned, feeding the characters in sequence to the character generator at the proper time during each scan.

Three dual 50-bit shift register IC's comprise the line memory. As with the page memory, the six registers operate in parallel and are equipped with feedback loops for recycling the stored data. Since the line memory storage capacity is exactly equal to the number of characters to be stored, however, no end-correction circuit is required.



(a) Dot patterns for characters "A" and "3"

(b) Character generator output codes for scan line 2 of characters "A" and "3"

Figure 3.6 Typical Display Pattern

During the first scan line for a new row, the characters to be displayed are transferred from the page memory to the line memory by clocking both memories simultaneously. The character generator produces no output during this first scan, so the previous characters stored in the line memory are clocked out without producing dots on the screen.

During each of the next seven scan lines, all 50 characters in the line memory are recycled and also fed to the character generator in succession. During the last two lines, which are dark, the memory contents are recycled, but the character generator is again instructed to produce no output.

The line memory control circuit passes clock pulses to the shift registers whenever characters are being entered or recycled. It includes a decade counter which keeps track of the scan line number. The counter output opens the memory input gate during the first scan line when data are to be entered from the page memory, and opens the output gate during those seven lines when the memory contents are fed to the character generator. The counter outputs are fed to the character generator as part of the code which determines the position of dots on the screen.

The line memory and control circuits are located on circuit card SC-B3.

Character Generator

The character generator is a read-only memory (ROM) custom precoded to store the dot patterns for 64 different characters. When supplied with the proper input codes, the memory outputs the dot pattern required for each character.

Since every character is produced by seven scan lines, the dot pattern in each line may be different, as shown in Figure 3.6a. The character generator must therefore be instructed not only what character to produce, but what scan line of that character is being generated. The character codes come in sequence from the line memory; the scan line number is supplied by the scan line counter in the line memory control circuit.

The characters are five dots wide. The ROM therefore provides five output bits, one for each dot. If a given bit is a "1", a dot is produced on the screen; if the bit is a "0", the space is left dark, as Figure 3.6b illustrates.

The first scan line is left dark by instructing the character generator to display line number zero. Since this line in the ROM is not programmed, no video output results regardless of the input data coming from the line memory. During the second scan line, the line memory again cycles and all 50 characters for the row being produced are fed to the character generator in sequence, along with the scan line number. As the character codes are fed in, the dot codes for the characters appear at the character generator output.

When the scan line is complete, the scan line counter increments, the memory is again cycled through all 50 characters, and the character generator produces the dot pattern for the third scan line. This process is repeated until the eighth scan line is complete. During the ninth and tenth scan lines, the character generator is again instructed to produce line zero. No video output results, and the last two lines are therefore dark.

Output Shift Register

The five dot code bits for each character appear in parallel at the character generator output. To produce dots at the proper time (and hence the proper position on the scan lines) however, the dot code bits must be fed in serial form to the video output circuits. A five-bit shift register performs the parallel-to-serial conversion.

Upon a command from the line memory control, the character generator output bits are loaded into the shift register. They are then clocked out of the register into the video combiner by pulses from

the master oscillator. After all five bits have been transferred and before the register is reloaded with the dot code for the next character, two extra clock pulses are allowed to pass. These extra pulses result in a blank space two dots wide between characters.

Video Circuitry

The dot code which comes from the character generator via the output shift register must be mixed with video synchronization and blanking signals and fed to the external monitor. The video circuits perform these functions.

A special large-scale IC contains all the circuits needed to produce the video synchronization and blanking pulses. Its input is driven at 1.008 MHz by a scaler which divides the master oscillator frequency by a factor of eight.

The sync generator outputs are shown in Figure 3.7. One horizontal sync pulse and one horizontal blanking pulse are produced for each of the 525 lines in a video field. One vertical blanking pulse is produced for each of the 60 fields scanned every second. Since standard television format uses interlace scanning, the blanking signals for alternate fields are offset from each other by one half of a horizontal scan time.

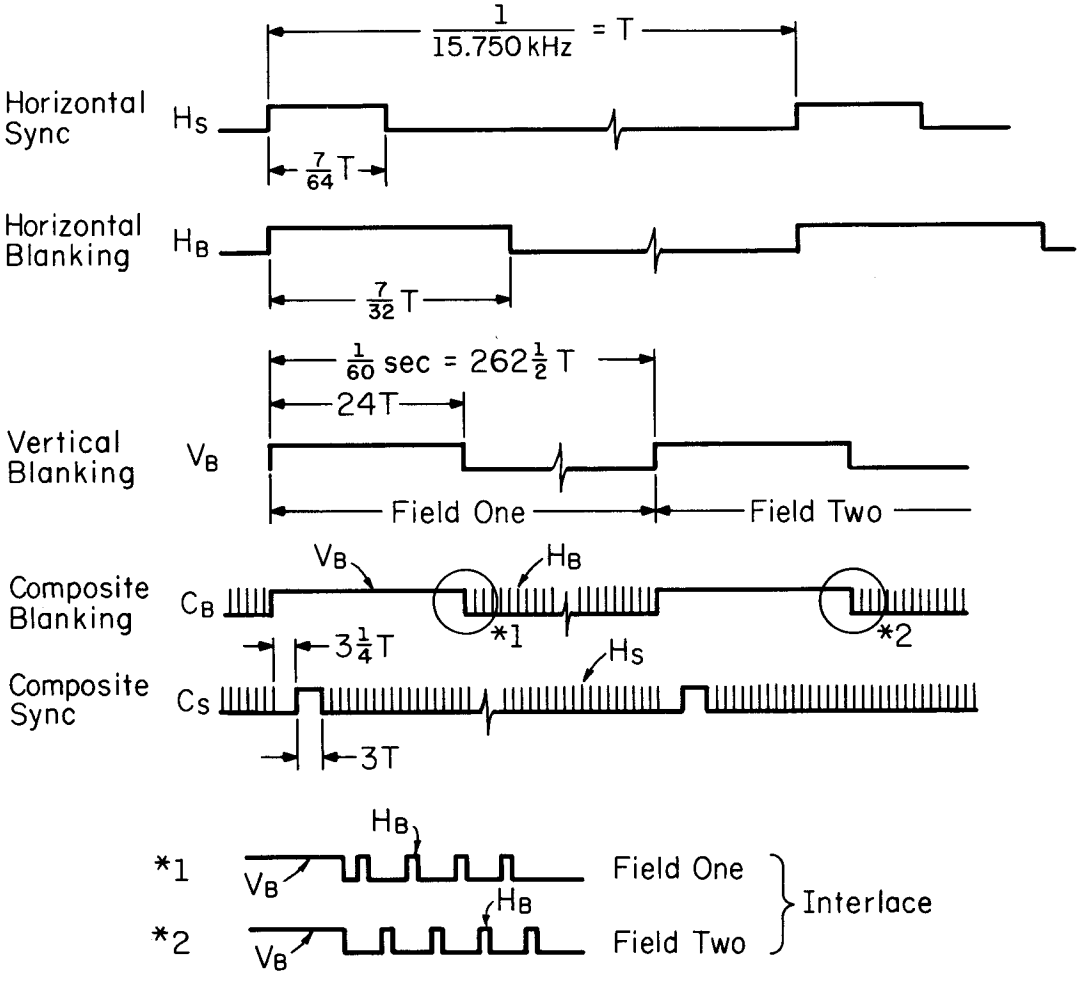


Figure 3.7 Video Timing Signals

The sync generator may be locked to an external timing source by providing a pulse to the reset terminal. Although this feature is not required for normal operation of the RVD-1002, the user may take advantage of it if he needs to synchronize the display with external devices. Consult the factory for further information.

The sync generator outputs are buffered by inverters and fed to the video combiner, as well as to the line and page memory controls, where they synchronize the memory cycles with the display fields.

The master oscillator and sync generator are located on circuit card SC-B1.

The video combiner mixes the video, blanking, and synchronization signals and drives the video monitor. The combiner is composed of three switched constant current sources, each of which is driven by one of the three input signals. The video monitor input impedance serves as a common load for all three current sources, so the output to the monitor is the sum of the three input signals. The contribution of each current source is adjustable by a potentiometer. Figure 1.4 shows the composite video waveform.

4. MAINTENANCE AND ADJUSTMENTS

Routine Maintenance

Your RVD-1002 requires very little routine maintenance. After an extended period of service the interior of the unit should be cleaned. Remove the top cover and gently pull the printed circuit boards from their connectors, remembering to note the location of each board. Clean all dust and foreign matter from the interior of the cabinet. Blow away any accumulations of dust on the circuit cards.

Check for corrosion of the connector fingers at the edge of the cards. If the contacts need cleaning, rub them with a clean cloth dampened in denatured alcohol. After the alcohol has evaporated, reinsert the cards in their proper connectors and replace the top cover. When inserting the cards, be sure to position the cards for proper finger to connector alignment.

Repair

Because the circuitry of the RVD-1002 is relatively complex, troubleshooting should be done only by an experienced technician who is familiar with high-speed digital circuitry. Isolating circuit problems in the unit requires, at the minimum, a calibrated, delayed-sweep oscilloscope having a bandwidth of 30 MHz or greater.

One simple test, however, is to measure the output voltages of the power supplies, as described later in this section.

In most cases, repairs can be obtained most easily and reliably by returning the unit to HAL Communications. Please notify the factory and wait to ship the unit until you have received a return authorization. Please note that the warranty is void if repairs are attempted by an unqualified person.

Adjustment

The internal controls of the RVD-1002 are adjusted at the factory for optimum performance and will normally not require further attention. If the unit is repaired, however, it is usually worthwhile to recheck the adjustments according to the procedure given in the following paragraphs. CAUTION: 115VAC is exposed inside the unit.

VOLTAGE ADJUSTMENTS

The output voltage ot the +5 volt, -5.5 volt, and -12 volt power supplies may be adjusted with the potentiometers on the power supply board (SC-B5) mounted toward the front of the cabinet. Consult the circuit board layout in Figure 7.5 for the location of these controls. The voltages may be measured at the "mother board" at the rear of the cabinet (the large circuit board by which the smaller boards are interconnected) or at the following pins on the power supply board connector:

Supply Voltage	Range	Connector Pin
+5 V	+4.9 to +5.2V	S (yellow)
−5.5V	−5.4 to −5.7 V	P (blue)
−12 V	−12.0 to −12.2 V	C (red)
−10 V	————	H (brown)
−15 V	————	J (orange)

The output voltages are set at the factory to provide best operation of the memory circuits. However, the output voltages should be set to fall within the range specified above. Note that the −10 volt and −15 volt supplies are not adjustable, but their outputs can be checked at the pins listed.

VIDEO ADJUSTMENTS

The sync level, setup level, and video level controls should be adjusted to obtain the waveform and voltages shown in Figure 1.4. Terminate the video output line with a 75-ohm resistive load and observe the output waveform with a calibrated oscilloscope having a bandwidth of 4 MHz or greater. The location of the three controls is shown in the circuit board layout, Figure 7.1. These adjustments are not critical.

5. USING A TELEVISION SET AS A MONITOR

Most standard American television sets can be easily modified to serve as video monitors. The change does not affect normal operation of the set.

CAUTION: Do not attempt to use as a monitor any television receiver in which one side of the AC line is connected to the chassis or circuit ground unless you supply AC power to the set from a reliable isolation transformer.

The modification is simply a matter of capacitively coupling the external video signal to the input of the first video amplifier stage. Figure 5.1 shows a typical transistorized video circuit. Although the component values and the biasing method may be slightly different in your set, the circuit will be essentially the same as the one shown. The video signal is injected at point A.

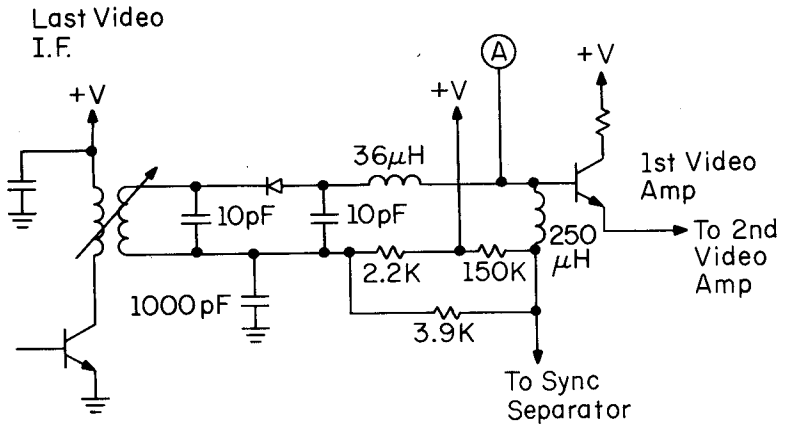


Figure 5.1 Typical Transistor Video Detector

The modified circuit is shown in Figure 5.2. Connect the negative end of a 150 ufd, 16 volt electrolytic capacitor to the base of the first video amplifier transistor. Mount a BNC connector on the cabinet as close as possible to the transistor. Using a short length of hookup wire, connect the center pin of the BNC connector to the positive end of the capacitor. If the distance is short, the capacitor leads themselves may take the place of the hookup wire. On the other hand, if the distance is greater than six inches, substitute a length of coaxial cable. Miniature coax, such as RG-174/U, may be used even though its characteristic impedance is 50 ohms.

Figure 5.3 shows a typical video circuit using tubes. The external video signal is injected at point A. Connect the negative end of a 10 ufd, 100 volt electrolytic capacitor to the detector side of the existing coupling capacitor, as shown in Figure 5.4. Note that a 75 ohm resistor is wired across the input connector to provide the proper load impedance for the RVD-1002 output.

Some tube-type sets may require a video level of 3 volts peak-to-peak to provide good contrast. In that case a two-stage video amplifier, such as that shown in Figure 5.5, may be inserted in the line from visual display system to the television set.

In some sets the video at the coupling point may have reverse polarity, with positive-going synchronization pulses and negative video information. This situation will often be found in transistorized sets which use a negative power supply and PNP transistors. The unity-gain phase inverter shown in Figure 5.6 may be inserted in the line from the RVD-1002 to reverse the video signal polarity.

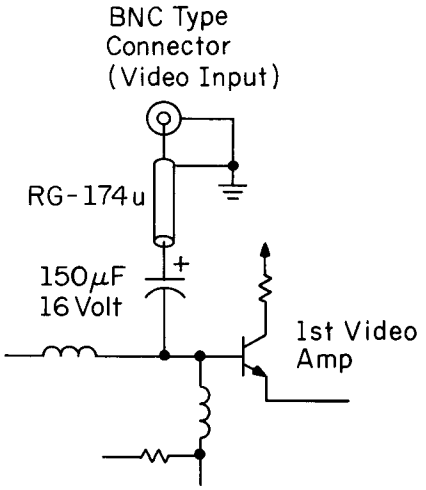


Figure 5.2 Modified Transistor Video Detector

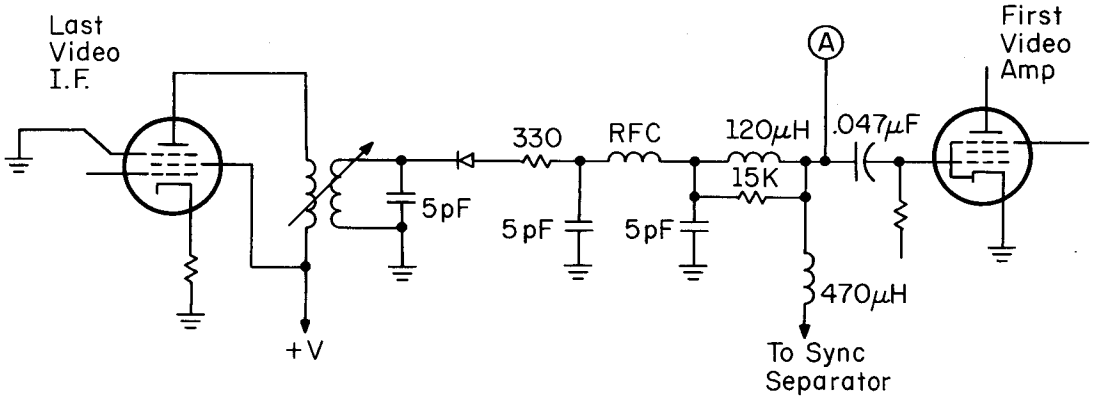


Figure 5.3 Typical Tube-type Video Detector

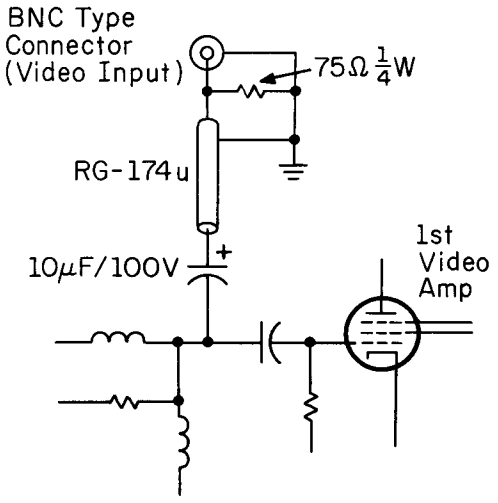


Figure 5.4 Modified Tube-type Video Detector

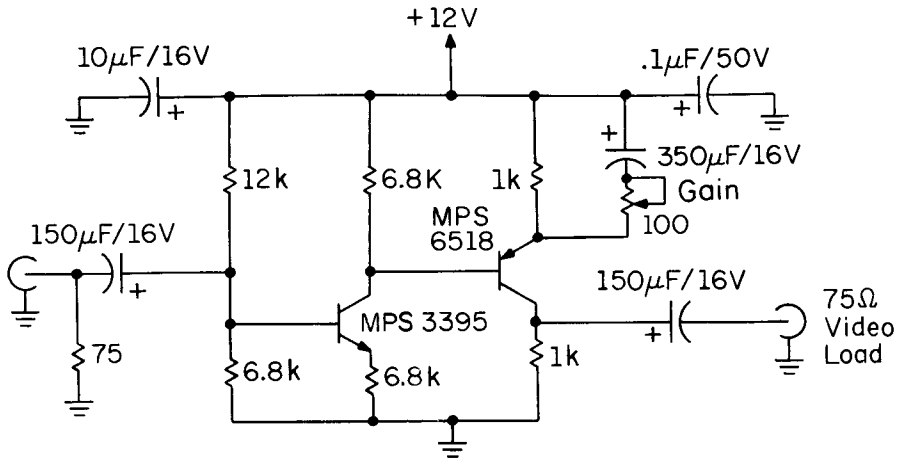


Figure 5.5 Video Amplifier

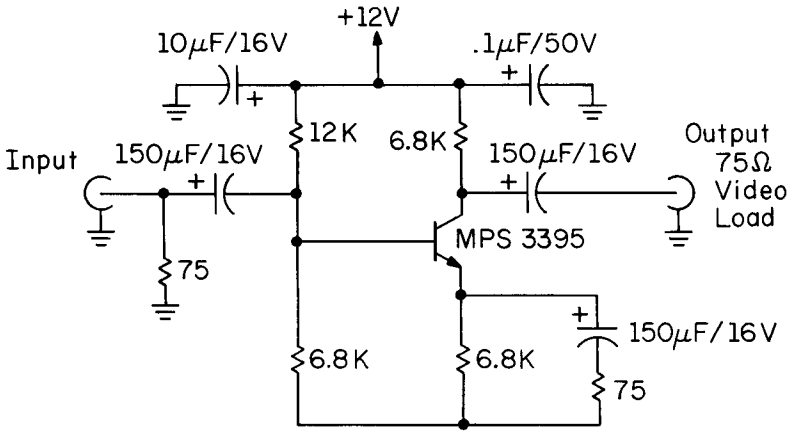
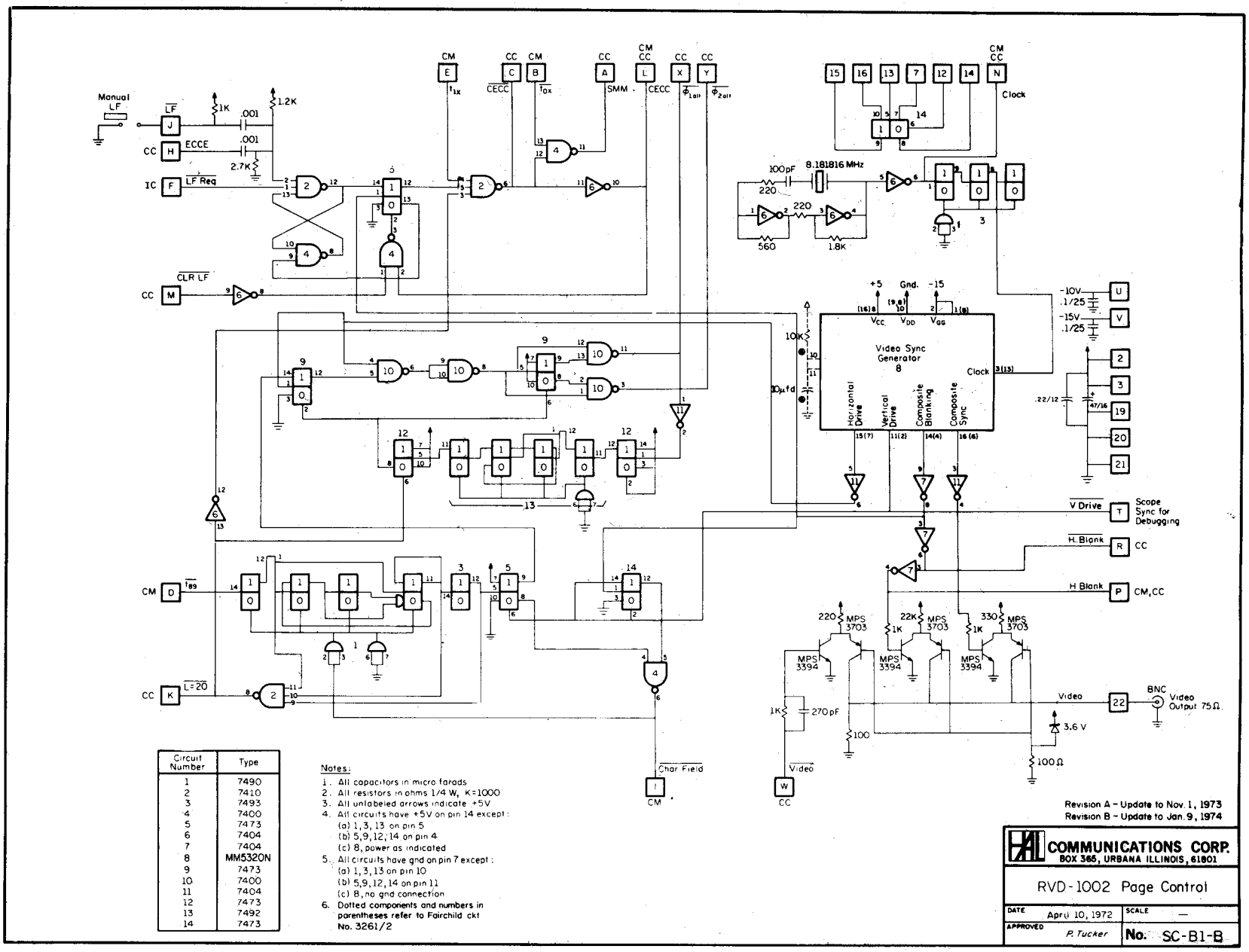


Figure 5.6 Video Inverter

6. SCHEMATIC DIAGRAMS

On the following pages are the schematic diagrams for the RVD-1002. Some connections within integrated circuits and other components are not shown in the diagrams.



Circuit Number	Type
1	7490
2	7410
3	7493
4	7400
5	7473
6	7404
7	7404
8	MM5320N
9	7473
10	7400
11	7404
12	7473
13	7492
14	7473

Notes:

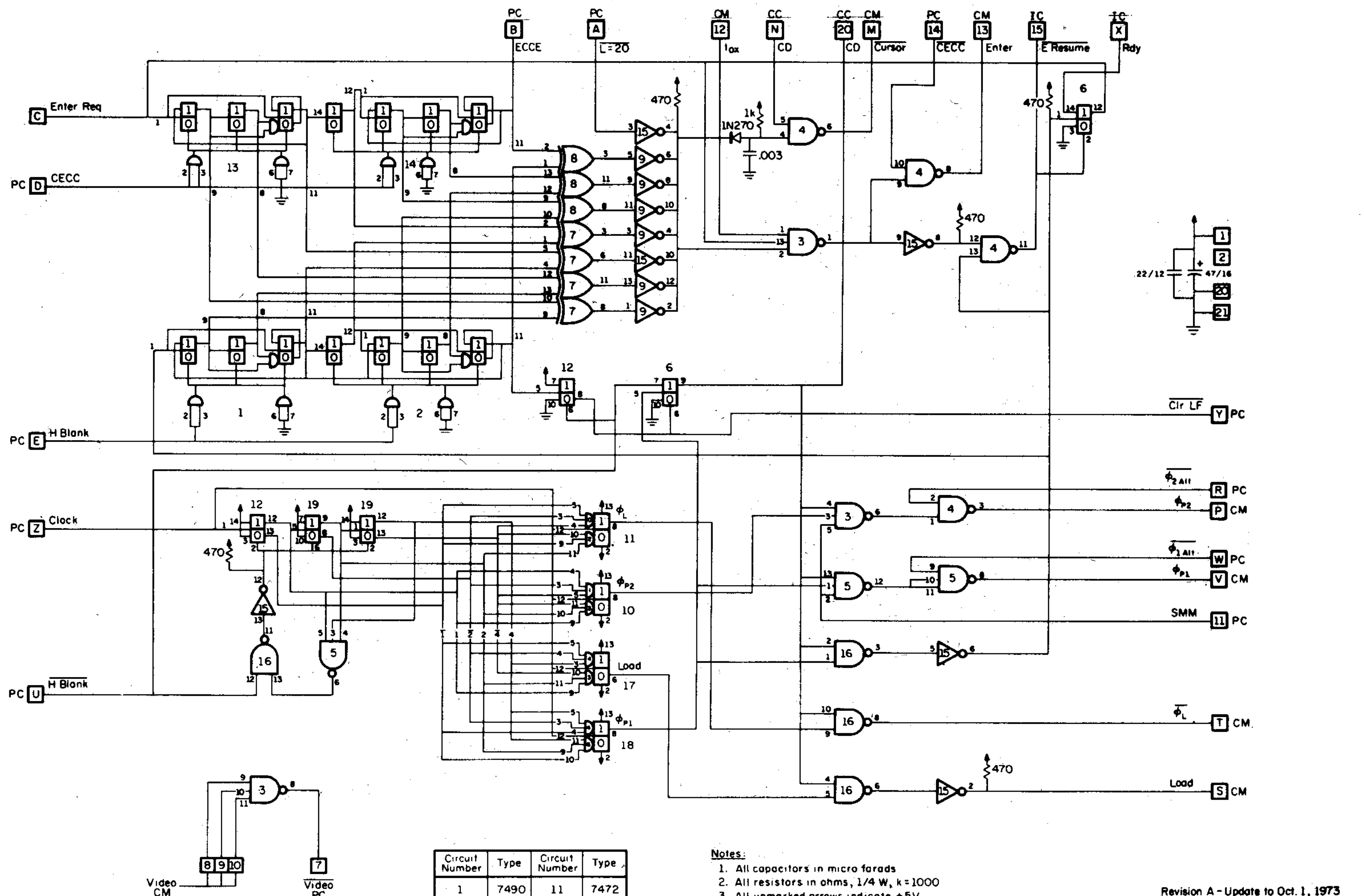
1. All capacitors in micro farads
2. All resistors in ohms 1/4 W, K=1000
3. All unlabeled arrows indicate +5V
4. All circuits have +5V on pin 14 except:
   (a) 1,3,13 on pin 5
   (b) 5,9,12,14 on pin 4
   (c) 8, power as indicated
5. All circuits have gnd on pin 7 except:
   (a) 1,3,13 on pin 10
   (b) 5,9,12,14 on pin 11
   (c) 8, no gnd connection
6. Dotted components and numbers in parentheses refer to Fairchild ckt No. 3261/2

Revision A – Update to Nov. 1, 1973
Revision B – Update to Jan. 9, 1974

HAL COMMUNICATIONS CORP.
BOX 365, URBANA ILLINOIS, 61801

RVD-1002 Page Control

DATE	April 10, 1972	SCALE	—
APPROVED	P. Tucker	No.	SC-B1-B



Circuit Number	Type	Circuit Number	Type
1	7490	11	7472
2	7490	12	7473
3	7410	13	7490
4	7400	14	7490
5	7410	15	7405
6	7473	16	7400
7	7486	17	7472
8	7486	18	7472
9	7405	19	7473
10	7472		

Notes:

1. All capacitors in micro farads
2. All resistors in ohms, 1/4 W, k=1000
3. All unmarked arrows indicate +5V
4. All circuits have +5V on pin 14 except:
   (a) 1,2,13,14 on pin 5
   (b) 6,12,19 on pin 4
5. All circuits have ground on pin 7 except:
   (a) 1,2,13,12 on pin 10
   (b) 6,12,19 on pin 11

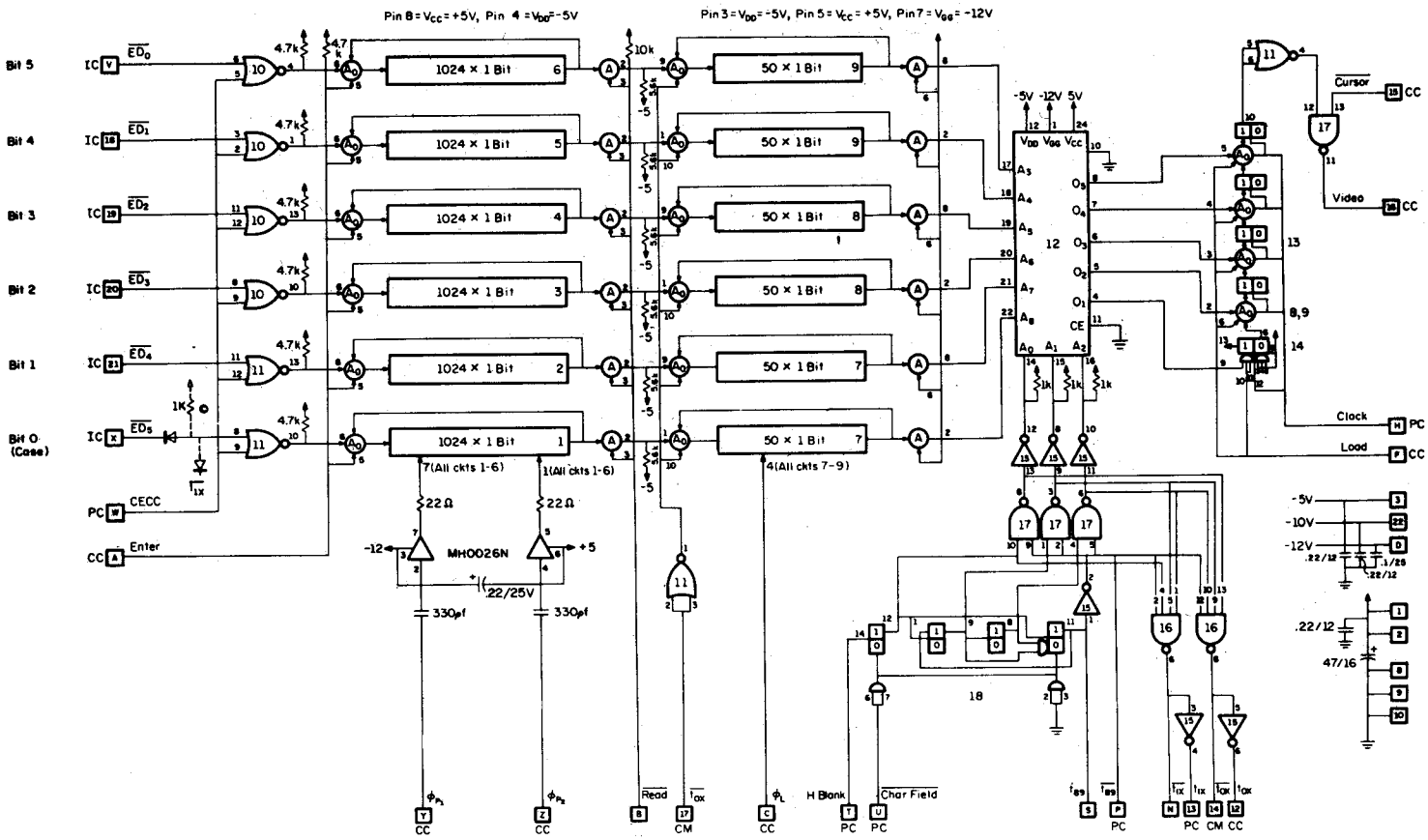
Revision A - Update to Oct. 1, 1973

HAL COMMUNICATIONS CORP.
BOX 365, URBANA ILLINOIS, 61801

RVD-1002 Character Control

DATE April 10, 1972 | SCALE —

APPROVED P. Tucker | No. SC-B2-A



Notes:

1. All capacitors in micro farads
2. All resistors in ohms, k = 1000 1/4 Watt
3. $\Rightarrow ac + b\bar{c} = d$
4. All unlabeled arrows indicate connections to +5 volts
5. Dotted components added for ASCII unit (RVD-1002A)
6. 2512 used interchangeably with 5013 or 2525
7. Circuit no.5 1-6 pins map as follows:

   5013 for 2525

   1-5 3-7

   2-6 4-8
8. 5.6k output resistors used with 2525 only

Circuit Number	Type	Circuit Number	Type
1	5013	10	7402
2	5013	11	7402
3	5013	12	2513
4	5013	13	7495
5	5013	14	7472
6	5013	15	7404
7	2509	16	7420
8	2509	17	7400
9	2509	18	7490

All circuits have +5 on pin 14 except:
(a) 1-9, 12 have power as noted
(b) 18 on pin 5

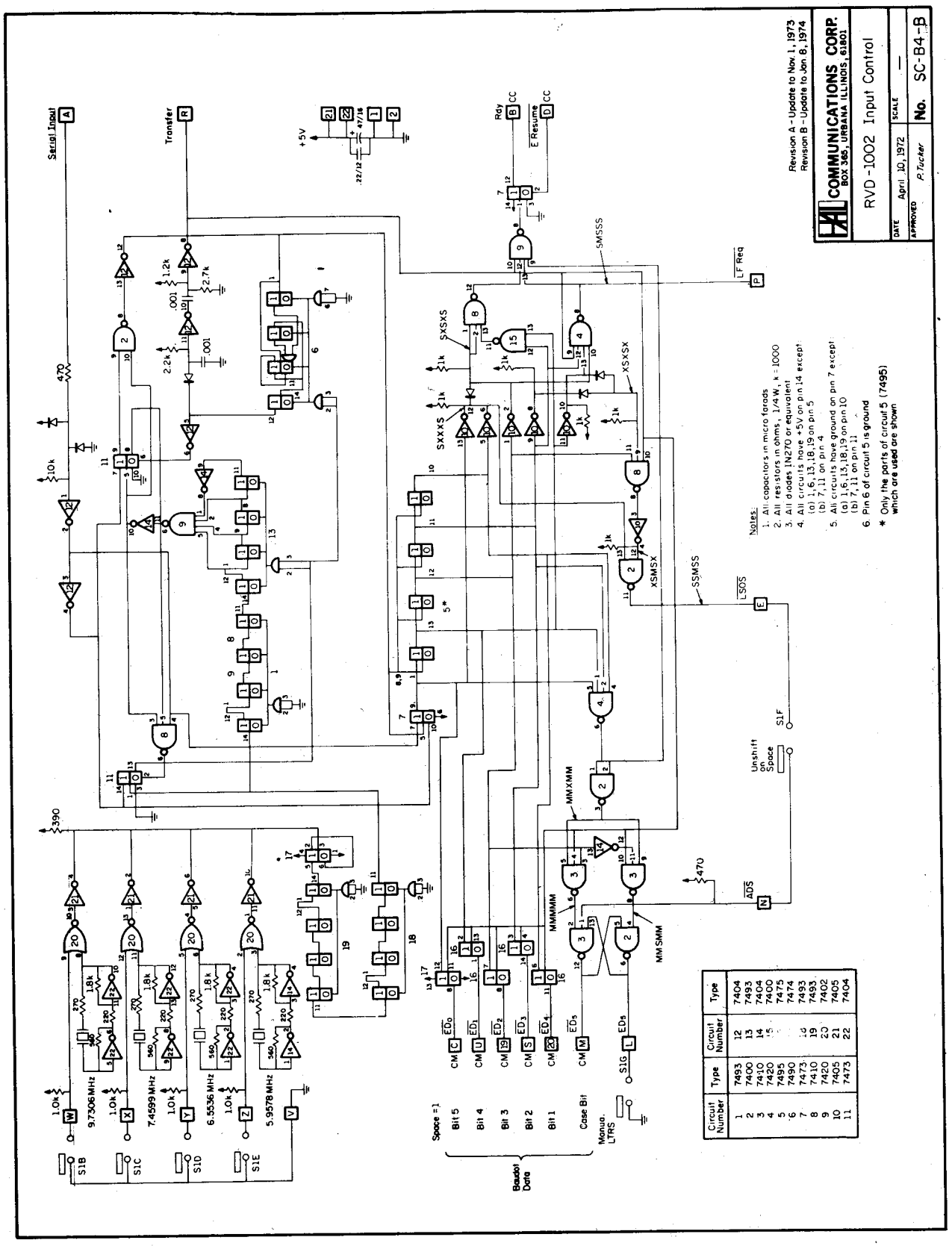
All circuits have ground on pin 7 except:
(a) 1-9, 12 have no ground connection
(b) 18 on pin 10

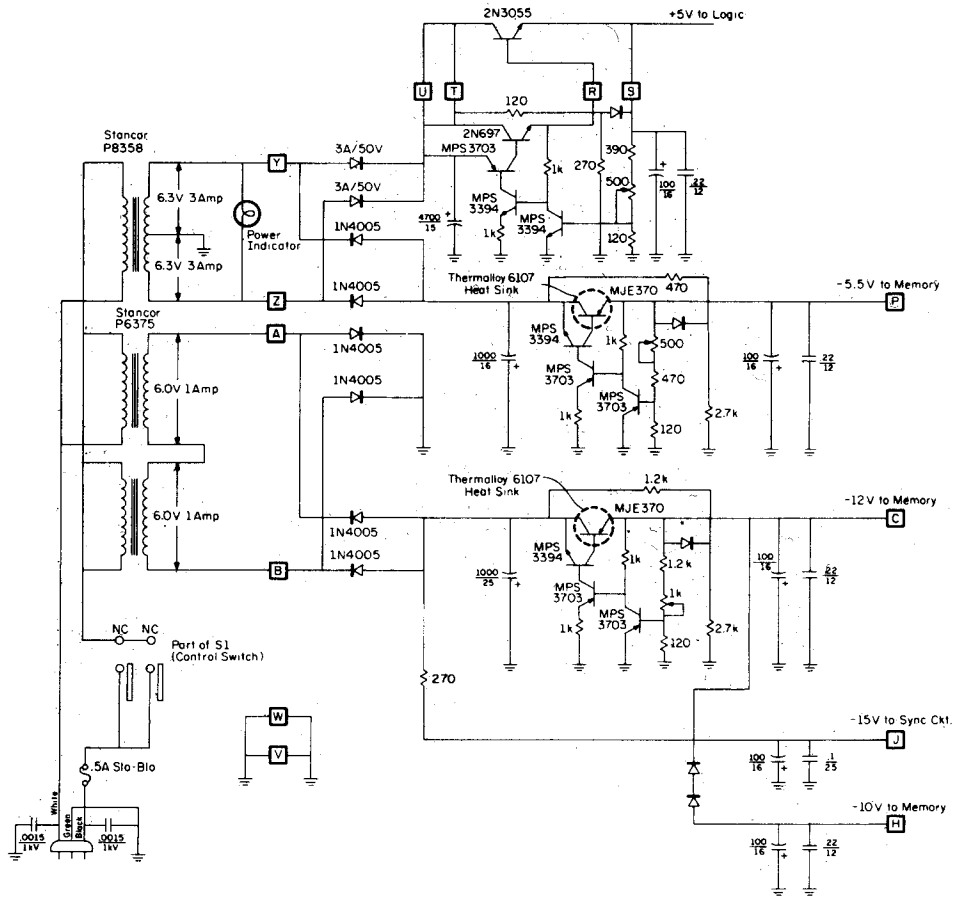
Revision A– Update to Nov. 1, 1973
Revision B– Update to Jan. 8, 1974

COMMUNICATIONS CORP.
BOX 365, URBANA ILLINOIS, 61801

RVD-1002 Character Memory

DATE	April 10, 1972	SCALE	—
APPROVED	P. Tucker	No.	SC-B3-B


COMMUNICATIONS CORP.
BOX 365, URBANA ILLINOIS, 61801
RVD-1002 Input Control
DATE April 10, 1972
SCALE —
APPROVED P. Tucker
No. SC-B4-B
Revision A - Update to Nov 1, 1973
Revision B - Update to Jan 8, 1974
Notes:
1. All capacitors in micro farads
2. All resistors in ohms, 1/4 W, k = 1000
3. All diodes IN270 or equivalent
4. All circuits have +5V on pin 14 except
(a) 1, 6, 13, 18, 19 on pin 5
(b) 7, 11 on pin 4
5. All circuits have ground on pin 7 except
(a) 1, 6, 13, 18, 19 on pin 10
(b) 7, 11 on pin 11
6. Pin 6 of circuit 5 is ground
* Only the parts of circuit 5 (7495) which are used are shown
Serial Input
Transfer
Rdy
E Resume
+5V
LF Req
SMSSS
SXSXS
SXXXS
XSXSX
XSMSX
SSMSS
LSOS
S1F
Unshift on Space
MMXMM
MMMMM
MMSMM
ADS
S1G
Case Bit
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Space = 1
Manua. LTRS
Baudot Data
9.7306 MHz
7.4599 MHz
6.5536 MHz
5.9578 MHz
S1B
S1C
S1D
S1E
Circuit Number | Type
1 7493
2 7400
3 7410
4 7420
5 7495
6 7490
7 7473
8 7410
9 7420
10 7405
11 7473
Circuit Number | Type
12 7404
13 7493
14 7404
15 7400
16 7475
17 7474
18 7493
19 7493
20 7402
21 7405
22 7404



Notes

1. All capacitances are in "micro farads / voltage rating"
2. All resistances are in ohms, k=1000, all are 1/4 Watt
3. All unmarked diodes are 1N4148 or equiv.
4. 2N3055 mounted on RVD-1002 chassis
5. Indicated supply voltages are nominal and are adjusted at factory to provide optimum performance.
6. CAUTION: Use of 117 V ac circuit with safety ground is recommended

Revision A - Update to Oct. 1, 1973

HAL COMMUNICATIONS CORP. BOX 365, URBANA ILLINOIS, 61801	
RVD-1002 Power Supply	
DATE April 10, 1972	SCALE —
APPROVED P. Tucker	No. SC-B5-A

7. PRINTED CIRCUIT CARD LAYOUTS

The following drawings show the position of components, conductors, and connectors on the printed circuit cards. Some late model changes may not be shown on these layouts.

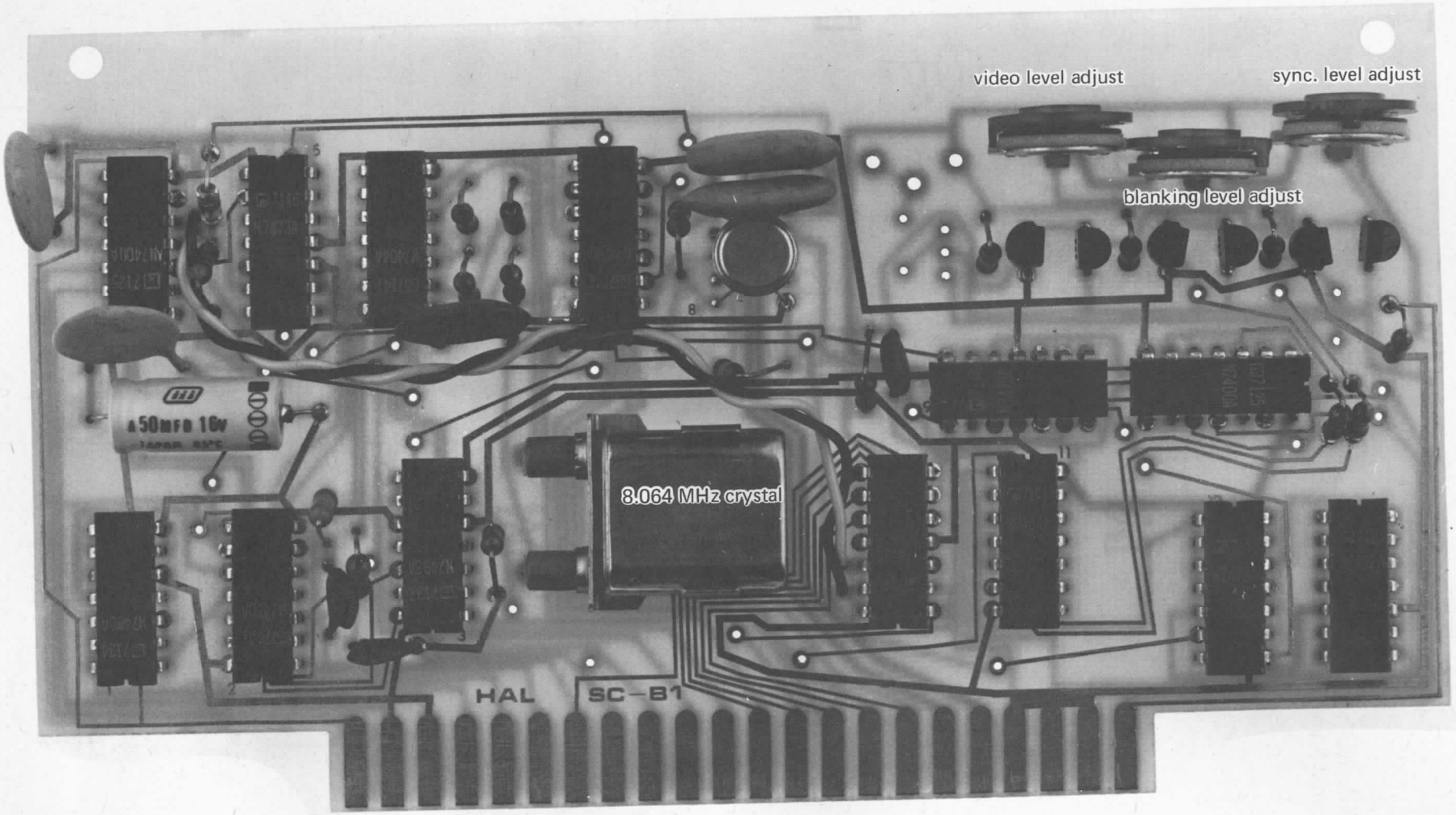


Figure 7.1
RVD-1002 SC-B1
Page Control Board

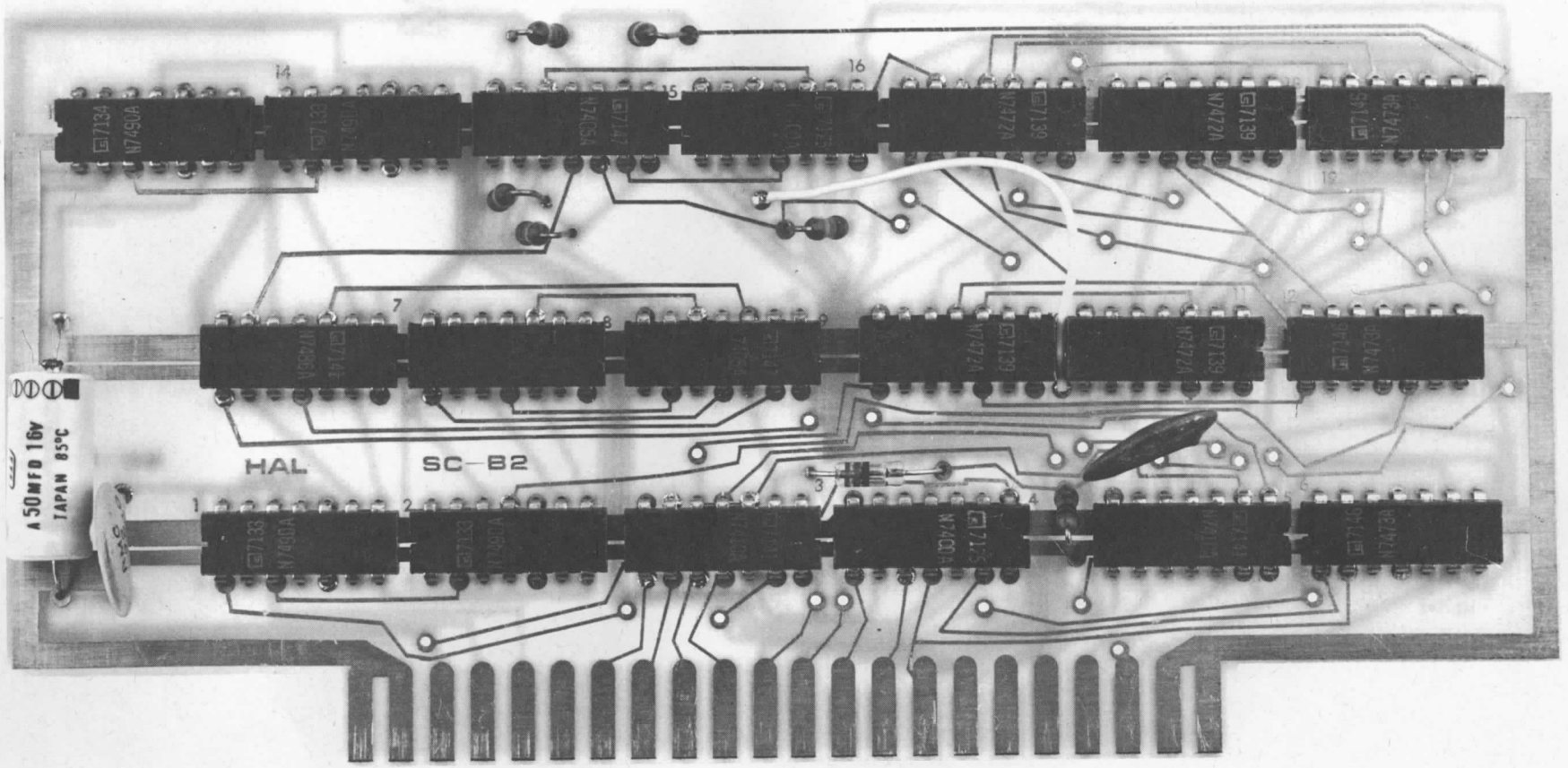


Figure 7.2
RVD-1002 SC-B2
Character Control Board

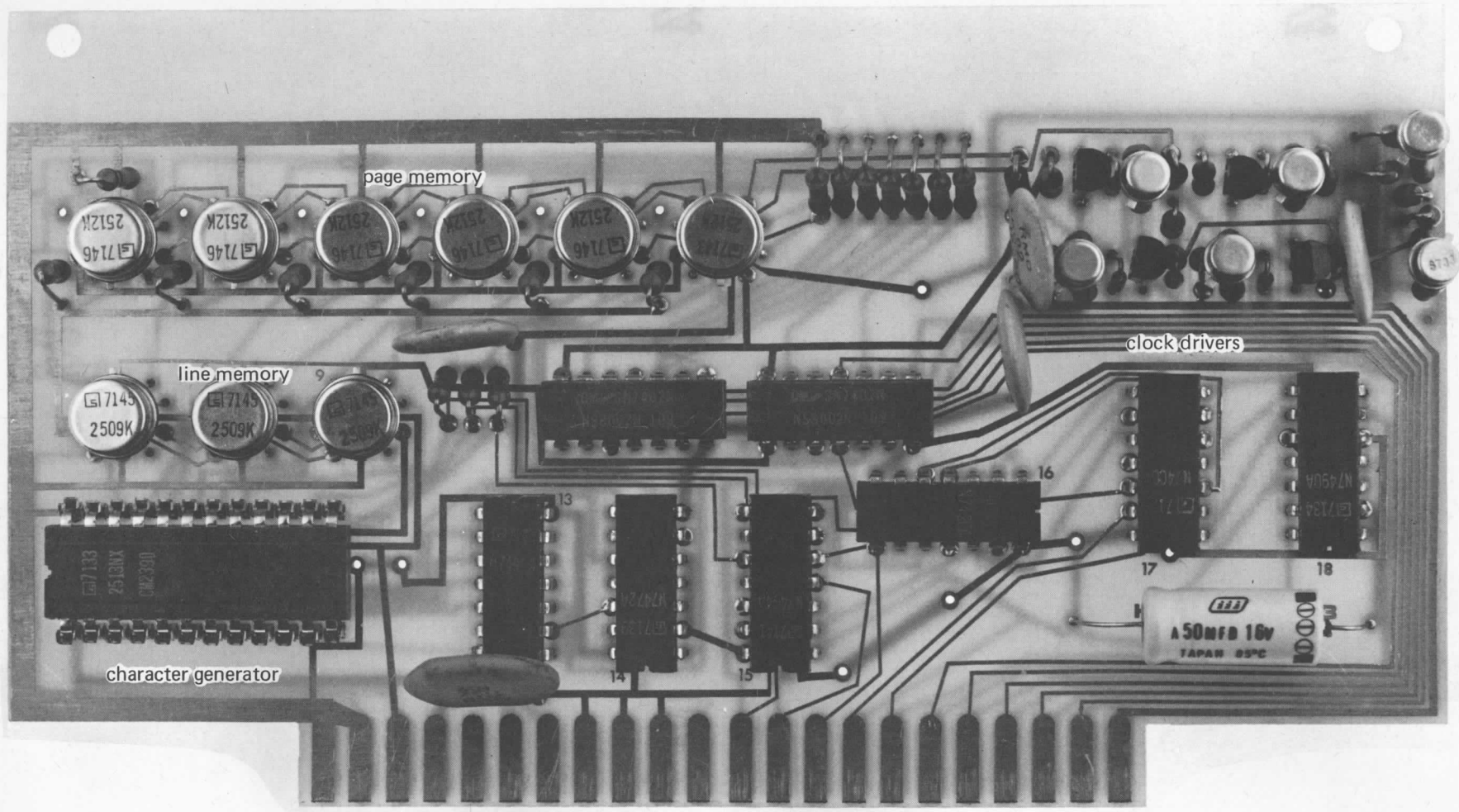


Figure 7.3
RVD-1002 SC-B3
Character Memory Board

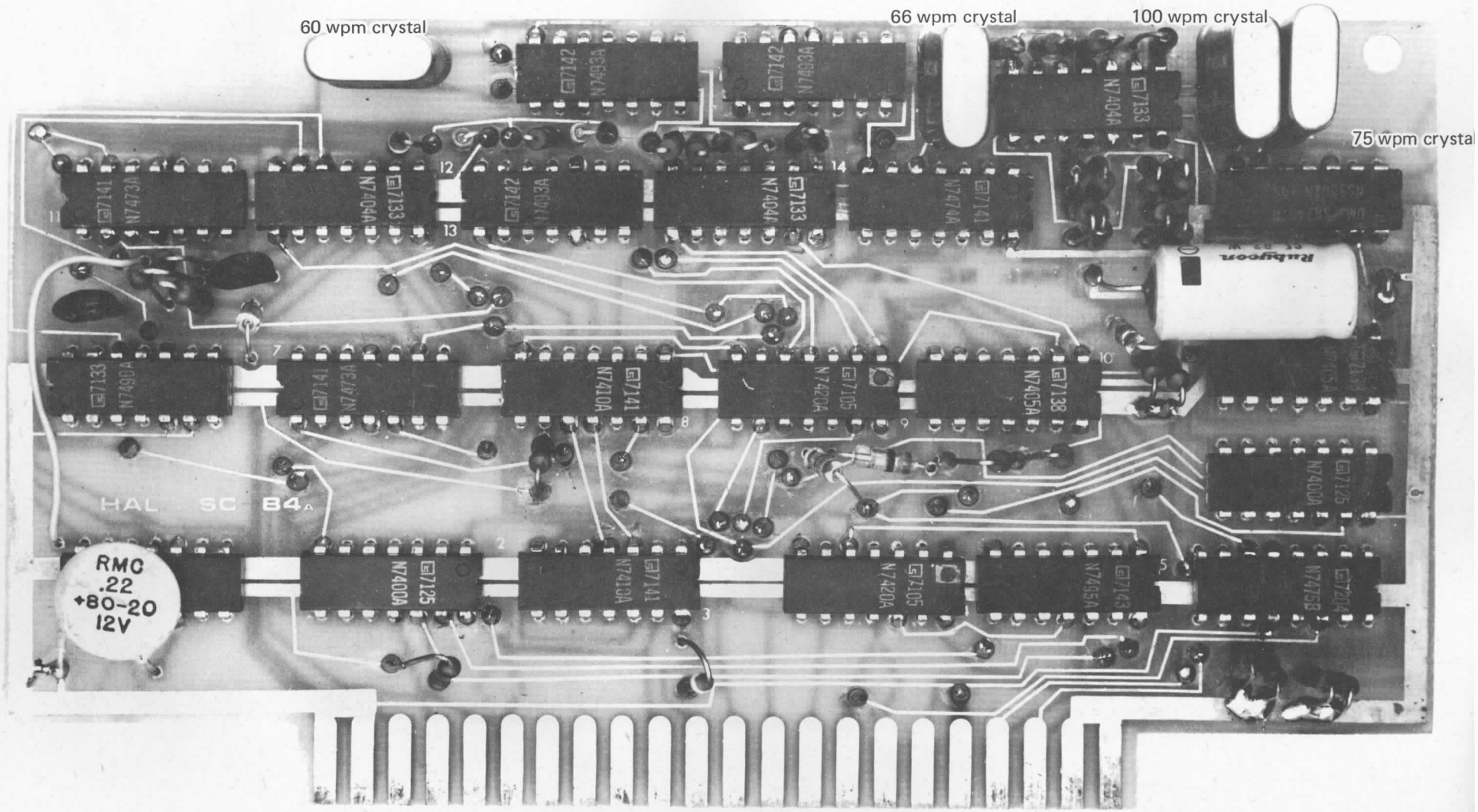


Figure 7.4
RVD-1002 SC-B4
Input Control

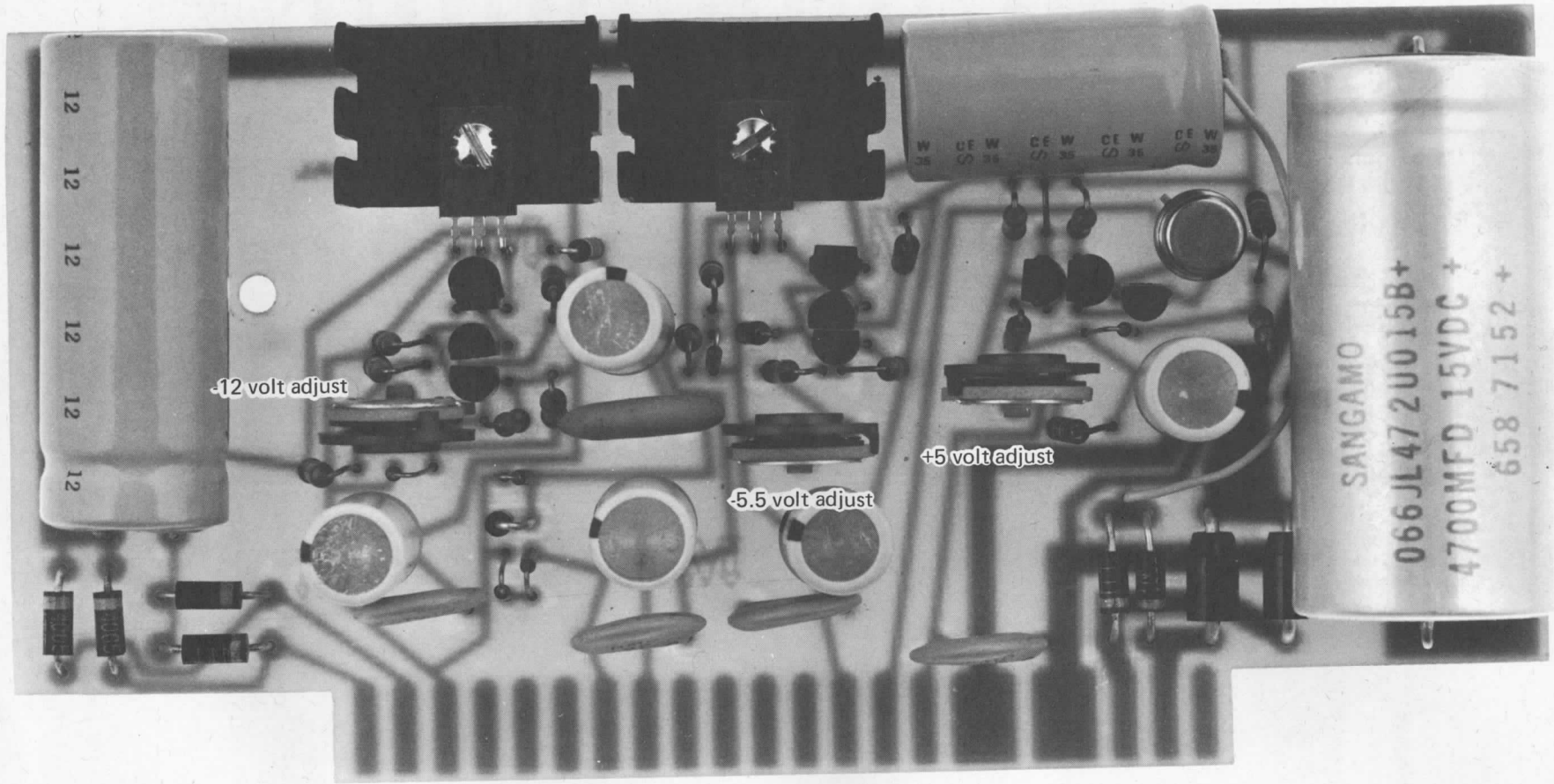


Figure 7.5
RVD-1002 SC-B5
Power Supply Board

8. PARTS LIST

RVD-1002 Main Chassis

1 - RVD-1002 Cabinet
1 - 8 position pushbutton switch with buttons
1 - 12v/35ma incandescent lamp assembly
1 - Stancor P-6375 or equivalent transformer
1 - Stancor P-8358 or equivalent transformer
1 - .01μfd/50v disc ceramic capacitor
2 - .001μfd/1kv disc ceramic capacitors
2 - 47μfd/16v disc ceramic capacitors
1 - 2N3055 power transistor
1 - UG-1094/u BNC coax connector
1 - 2 circuit ¼" phone jack
4 - Cinch-Jones 50-44-S-20 edge connector
1 - Cinch-Jones 50-44-A-30 edge connector
1 - Buss HKP fuse holder
1 - Line cord, 6'
1 - .5ASB MDL fuse
1 - Line cord strain relief
1 - TO-3 heat sink for 2N3055
2 - Angle bracket
1 - 7 Terminal Tie Strip
1 - 6 Terminal Tie Strip
1 - 3/8" hole plug

1 -	SC-B1	Printed Circuit Board
1 -	SC-B2	Printed Circuit Board
1 -	SC-B3	Printed Circuit Board
1 -	SC-B4	Printed Circuit Board
1 -	SC-B5	Printed Circuit Board
1 -	SC-MB	Printed Circuit Board
8 -	4-40 x 5/16"	Threaded Standoff
2 -	2-56 x ½"	Flathead screw
2 -	2-56	Nuts
10 -	4-40 x ¼"	Machine screw
2 -	4-40	Nuts
12 -	4-40	Lockwasher
12 -	6-32 x ¼"	Machine Screw
13 -	6-32	Nut
12 -	6-32	Lockwasher
1 -	#6	Ground Solder lug
1 -	3/8"	Ground Solder lug

RVD-1002 SC-B1 Page Control Board

Resistors (¼ watt, 10%)
1 - 100 ohms
2 - 220
3 - 330
1 - 560
3 - 1000
1 - 1200
1 - 1800
1 - 2700
1 - 4700
1 - 100K
3 - 1000 ohm trimpot (IRC)

Semiconductors
1 - 1N270
3 - MPS3394
3 - MPS3703

Miscellaneous
1 - 8.064 MHz .01% crystal
1 - Crystal Socket (Augat)

Capacitors (μfd)
1 - 100 pf/500V disc ceramic
1 - 270 pf/500V disc ceramic
2 - .001/1KV disc ceramic
1 - .01/50V disc ceramic
2 - .1/25V disc ceramic
2 - .22/12V disc ceramic
1 - 47/16V electrolytic

Integrated Circuits
2 - 7400
3 - 7404
1 - 7410
4 - 7473
1 - 7490
1 - 7492
1 - 7493
1 - HSUB0525

8. PARTS LIST, CONT.

RVD-1002 SC-B2 Character Control Board

Resistors (¼ watt, 10%)
5 - 470 ohm
1 - 1000

Capacitors (μfd)
1 - .003/500V disc ceramic
1 - .22/12V disc ceramic
1 - 47/16V electrolytic

Semiconductors
1 - 1N270

Integrated Circuits
2 - 7400
2 - 7405
2 - 7410
3 - 7473
4 - 7472
2 - 7486
4 - 7490

RVD-1002 SC-B3 Character Memory Board

Resistors (¼ watt, 10%)
2 - 2.2 ohm
10 - 100
5 - 1000
7 - 4700
6 - 5600
1 - 10K

Semiconductors
8 - 1N4148
6 - 40637
4 - MPS6518

Capacitors (μfd)
1 - .1/25V disc ceramic
3 - .22/12V disc ceramic
1 - 47/16V electrolytic

Integrated Circuits
1 - 7400
2 - 7402
1 - 7404
1 - 7420
1 - 7472
1 - 7490
1 - 7495
3 - 2509
6 - 2512
1 - 2513NX/CM2390

8. PARTS LIST, CONT.

RVD-1002 SC-B4 Input Control

Resistors (¼ watt, 10%)
4 - 220 ohm
4 - 270
1 - 390
2 - 470
4 - 560
10 - 1000
1 - 1200
4 - 1800
1 - 2700

Semiconductors
6 - 1N270

Miscellaneous
1 - 9.7306 MHz crystal
1 - 7.4599 MHz crystal
1 - 6.5536 MHz crystal
1 - 5.9578 MHz crystal

Capacitors (μfd)
2 - .001/KV disc ceramic
1 - .22/12V disc ceramic

Integrated Circuits
2 - 7400
1 - 7402
3 - 7404
2 - 7405
2 - 7410
2 - 7420
2 - 7473
1 - 7474
1 - 7475
1 - 7490
4 - 7493
1 - 7495

RVD-1002 SC-B5 Power Supply Board

Resistors (¼ watt, 10%)
3 - 120 ohm
1 - 270
1 - 390
2 - 470
6 - 1000
3 - 1200
2 - 2700
2 - 500 ohm trimpot (IRC)
2 - 1000 ohm trimpot (IRC)

Miscellaneous
2 - Heat sink
2 - 4-40 x 3/8" screw
2 - 4-40 nut
2 - 4-40 lockwasher

Capacitors (μfd)

1 - .1/25V	disc ceramic
4 - .22/12V	disc ceramic
5 - 100/16V	electrolytic
1 - 1000/16V	electrolytic
1 - 1000/25V	electrolytic
1 - 4700/16V	electrolytic

Semiconductors

2 - 50 PIV/3A	Rectifier
6 - 1N4005	Rectifier
1 - 1N4729	Zener
6 - 1N4148	Signal diode
2 - MJE370	
1 - 2N697	
5 - MPS3703	
4 - MPS3394	