This plot shows the Pixel-Planes 4.1 chip, designed in 1985 and fabricated in 3-micron NMOS technology through the MOSIS chip foundry. The chip contains 128 SIMD pixel processors each with 72 bits of memory, along with a parallel linear expression evaluator that supported most of its graphics rendering calculations. 2,048 of these chips, operating at 8MHz, were used to build the ‘smart’ frame buffer in the Pixel-Planes 4 machine, which operated in the UNC-CS Graphics Lab from 1986 until about 1991. The machine was demonstrated at SIGGRAPH ’86 and was the fastest general-purpose graphics system in the world at that time.

This is a plot of the Pixel-Planes 5 Enhanced Memory Chip (EMC) fabricated in 1989 in 1.6-micron CMOS technology. The chip contains 256 SIMD bit-serial pixel processors each with 208 bits of memory, operating at 40MHz. The chip also implemented a parallel quadratic expression evaluator that calculated Ax + By + C + Dx2 +Exy + Fy2 in parallel for all pixels. The chip formed the heart of the rendering processor on the Pixel-Planes 5 parallel computer, which became operational in 1989 and was demonstrated at SIGGRAPH ’92. Like its predecessor, Pxpl5 was the fastest and most versatile general-purpose graphics system in the world for some years, achieving an unprecedented 1M smooth-shaded polygons/sec rendering rates. A large multi-rack Pixel-Planes 5 system was in continuous operation in the CS Department’s Graphics Lab until its decommissioning September 1997.