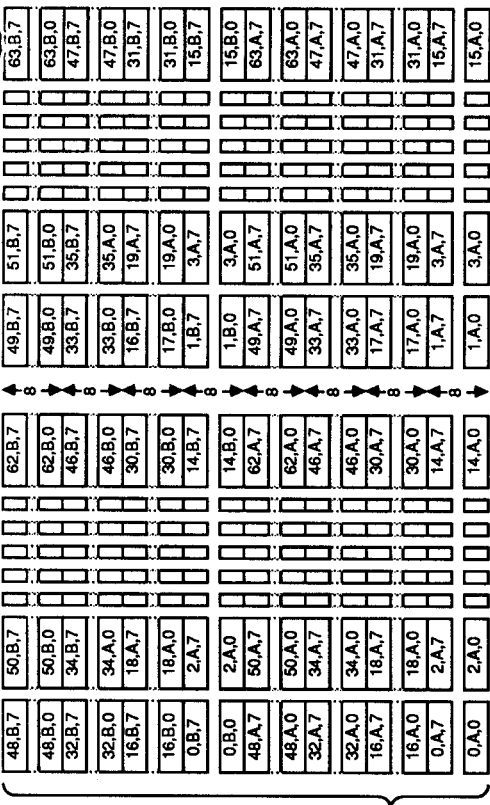


Layout divides EMCs & VRAMs into 4 banks, numbered 0-3, each bank containing 16 EMCs & 16 VRAMs. All 16 EMCs ^{millions} driven by one set of drivers, 16 VRAMs ~~driven by one set of drivers~~ divided into A/B for clocks.

Banks A0, A1, A2, A3
B0, B1, B2, B3



Screen Organization for 1 Renderer, with 128x128 pixel processors.

Message formats at various points in the corner turning process. Pixels are accessed in scan-line order.

Number refers to VRAM index (same as EMC index).

