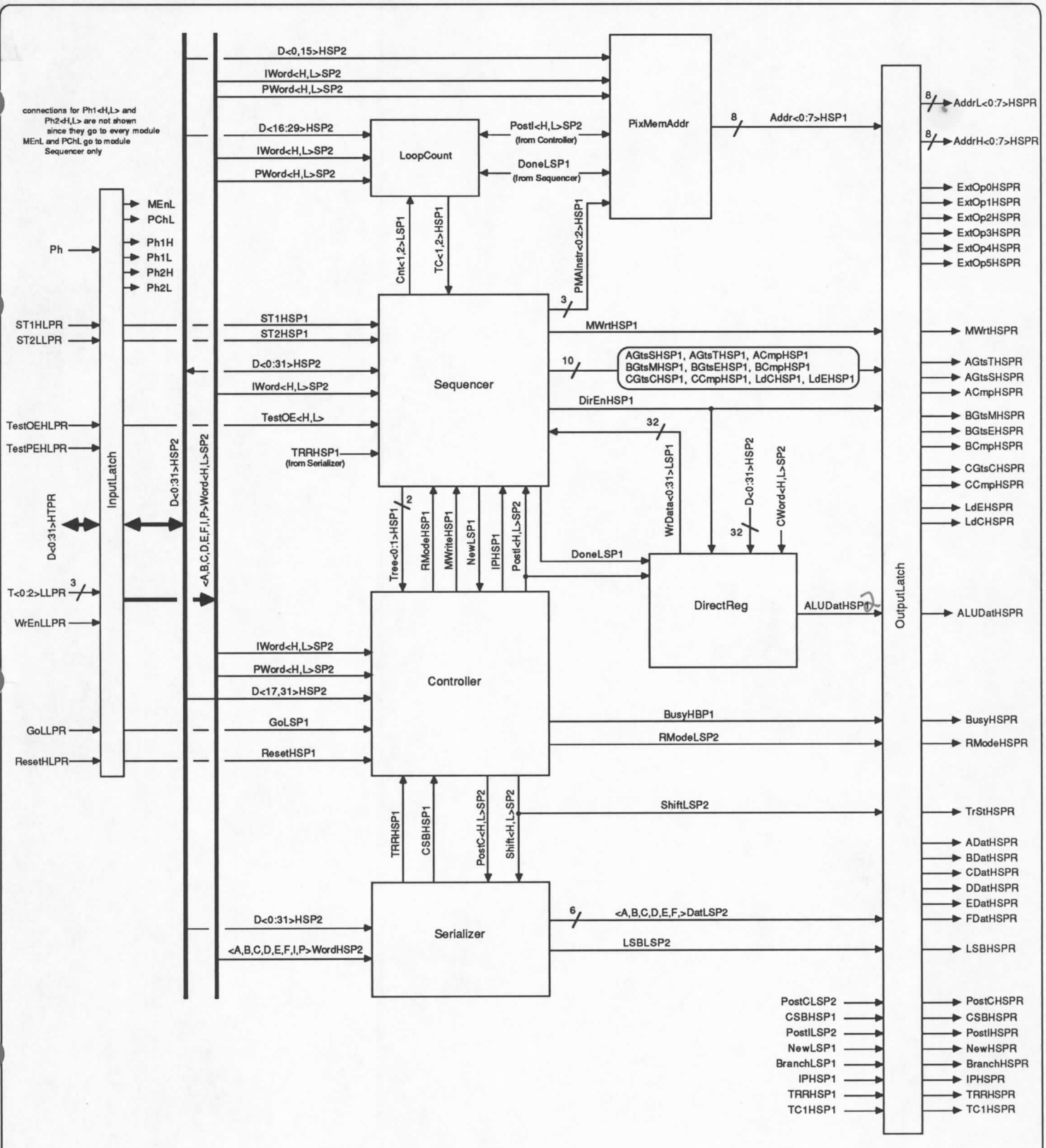
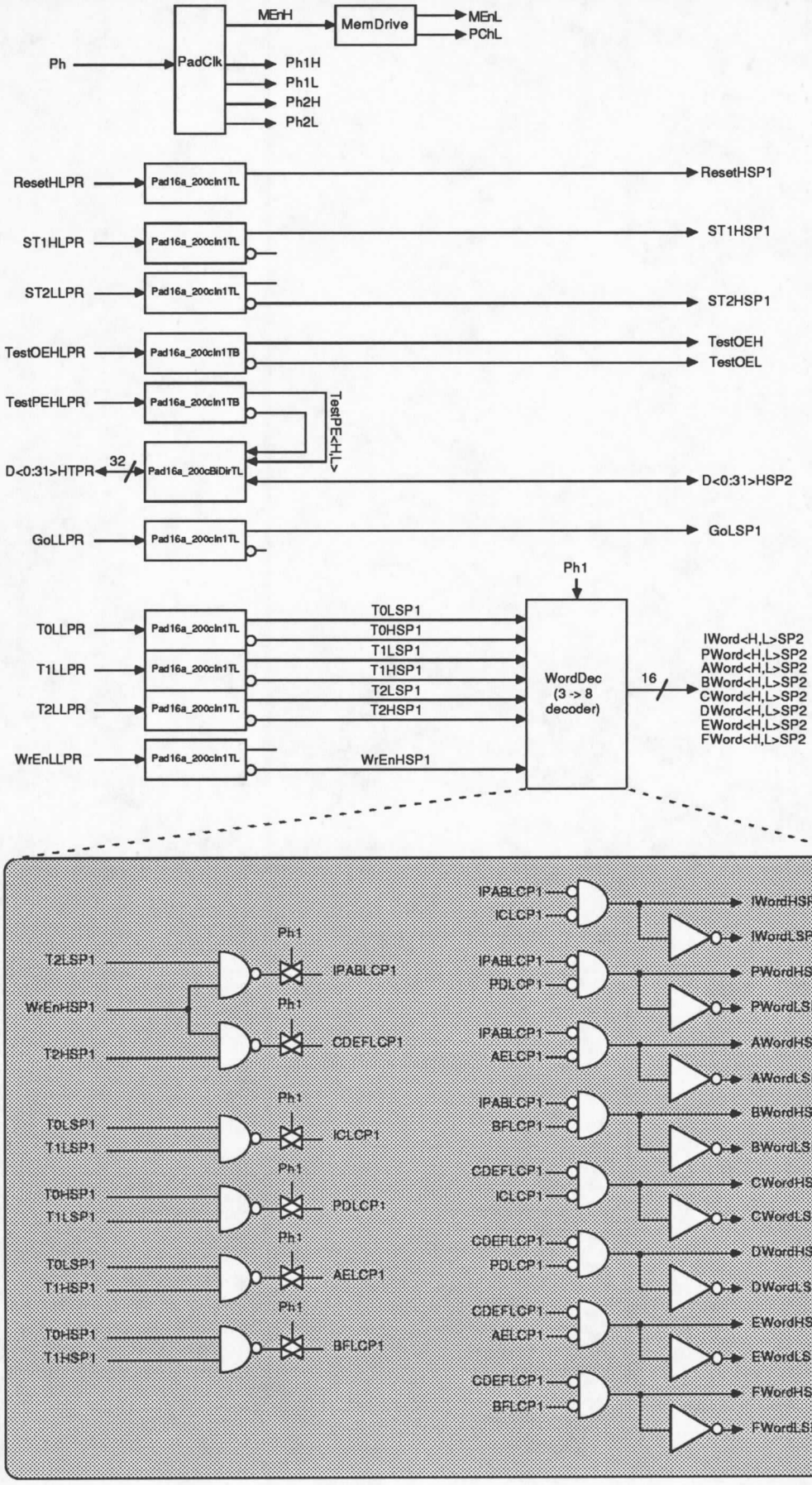


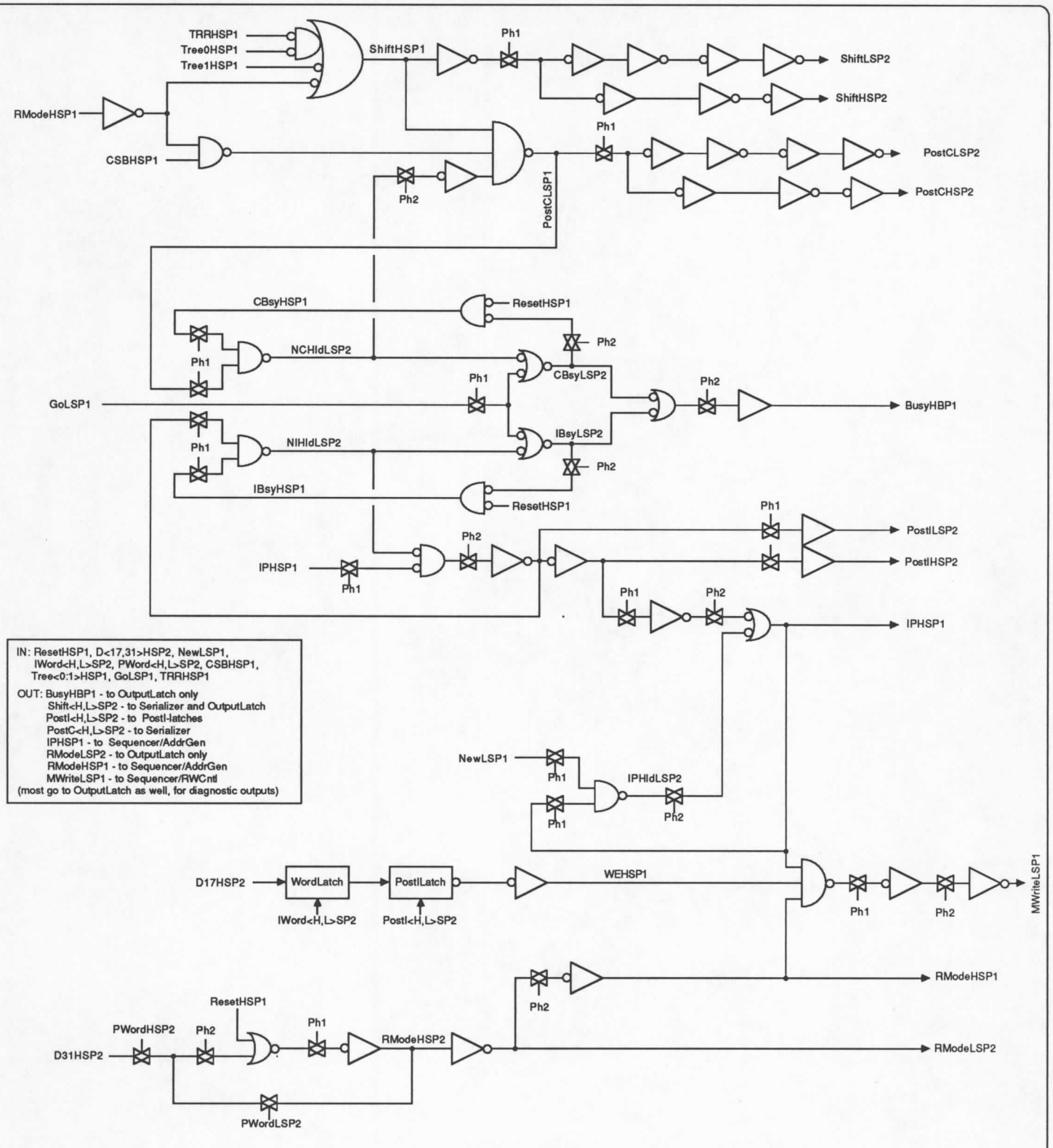
Block Diagram of Image Generation Controller

jge/21-Jul-89



InputLatch module

jge/24-May-89

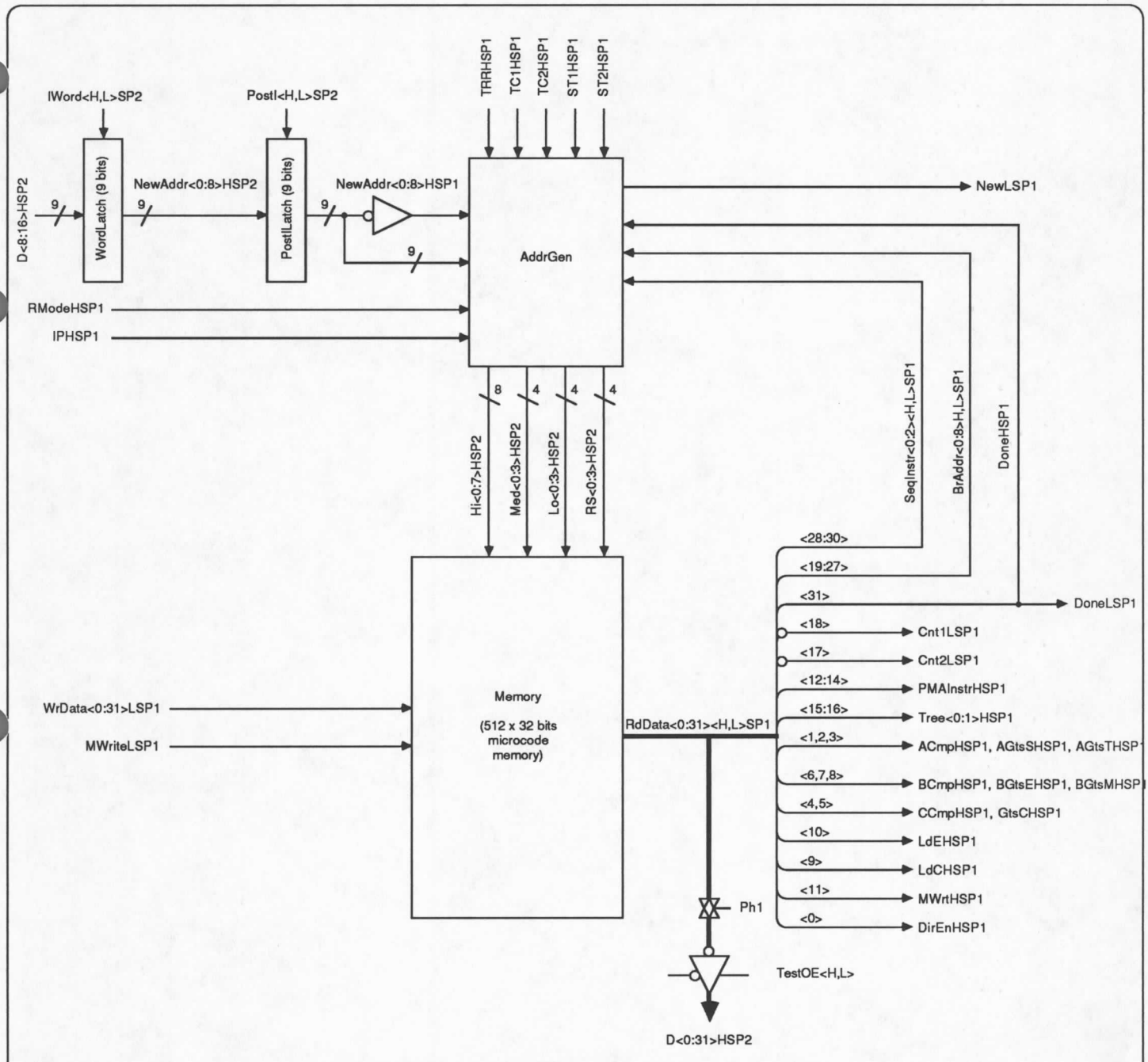


IN: ResetHSP1, D<17,31>HSP2, NewLSP1,
IWord<H,L>SP2, PWord<H,L>SP2, CSBHSP1,
Tree<0:1>HSP1, GoLSP1, TRRHSP1

OUT: BusyHBP1 - to OutputLatch only
Shift<H,L>SP2 - to Serializer and OutputLatch
PostI<H,L>SP2 - to PostI-latches
PostC<H,L>SP2 - to Serializer
IPHSP1 - to Sequencer/AddrGen
RModeLSP2 - to OutputLatch only
RModeHSP1 - to Sequencer/AddrGen
MWriteLSP1 - to Sequencer/RWCntl
(most go to OutputLatch as well, for diagnostic outputs)

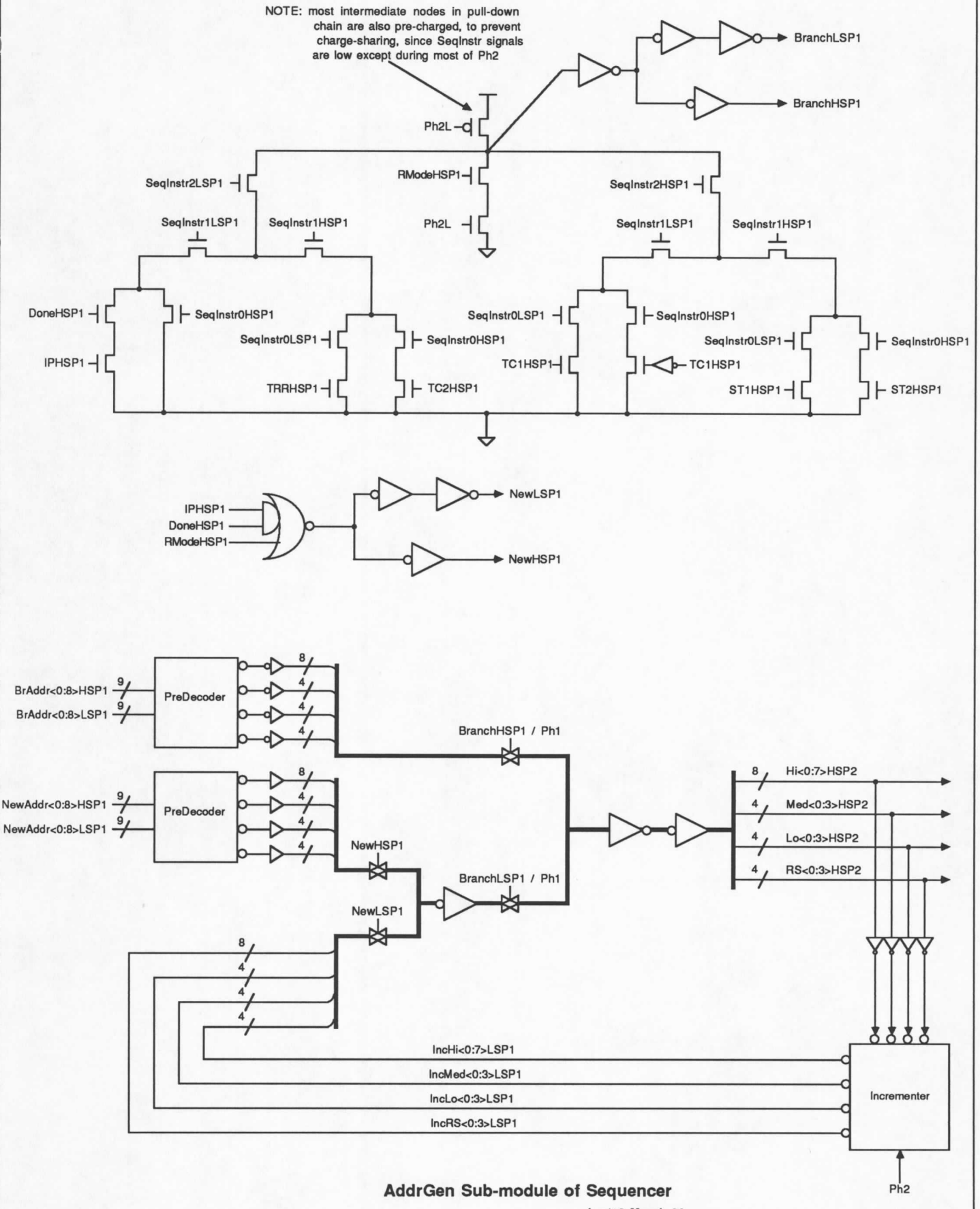
Controller Module

jge/1-May-89



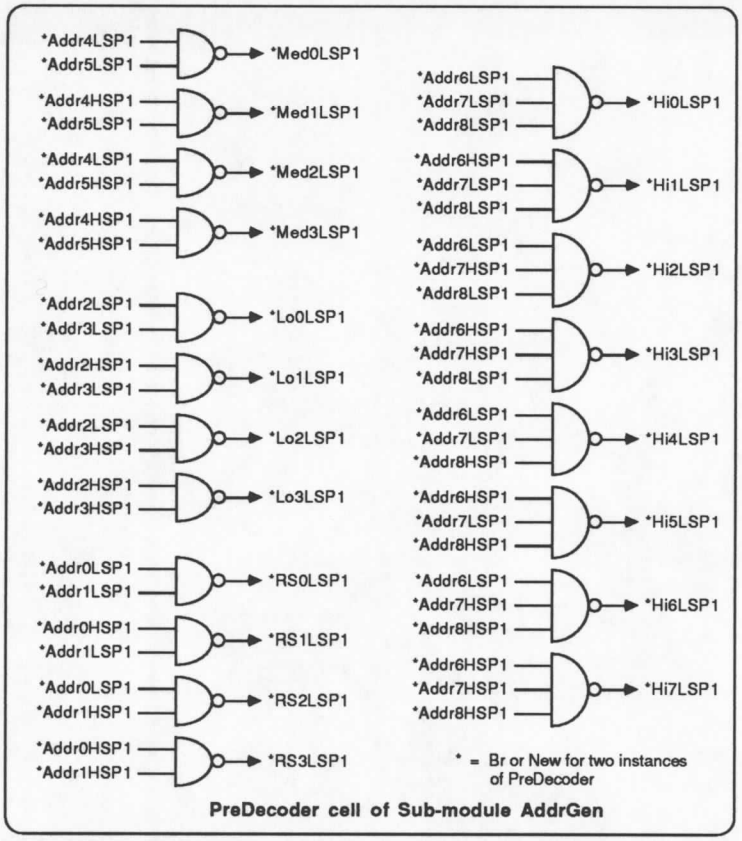
Block Diagram of Sequencer module

jge/1-May-89

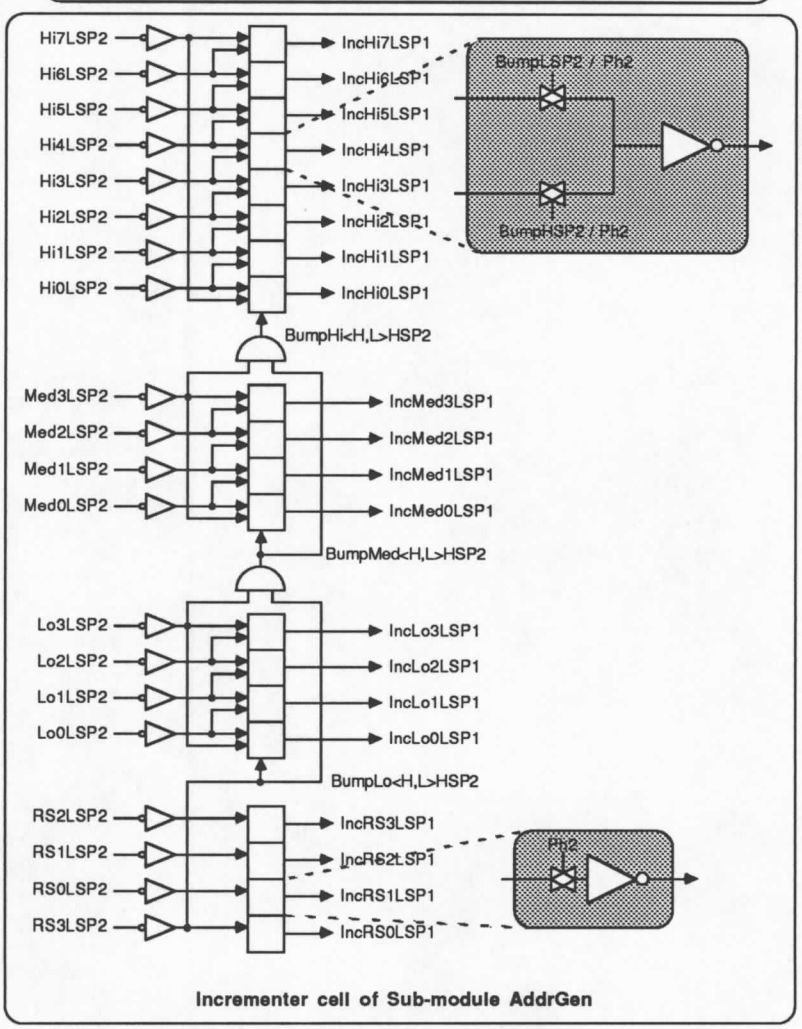


AddrGen Sub-module of Sequencer

jge/16-March-89

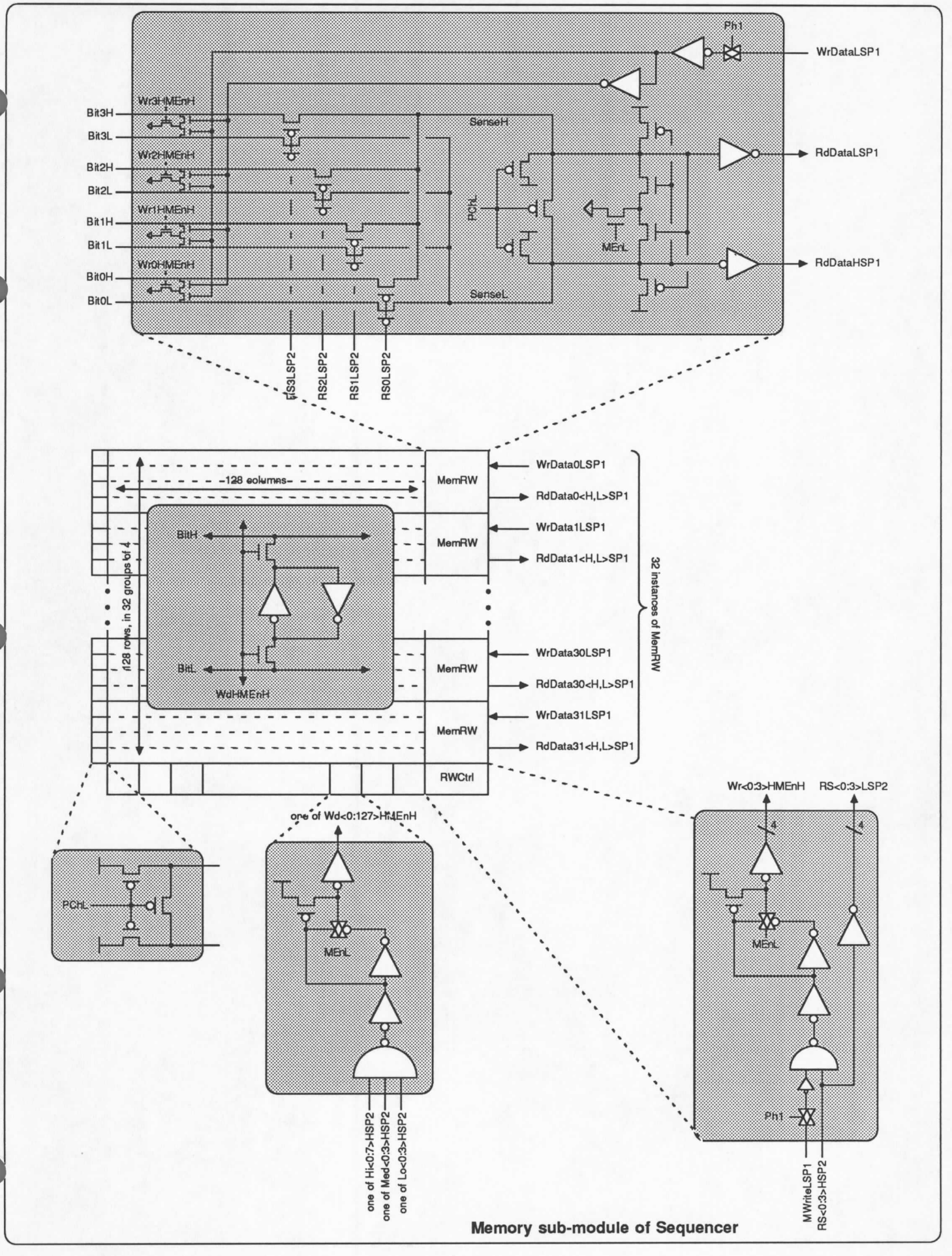


PreDecoder cell of Sub-module AddrGen

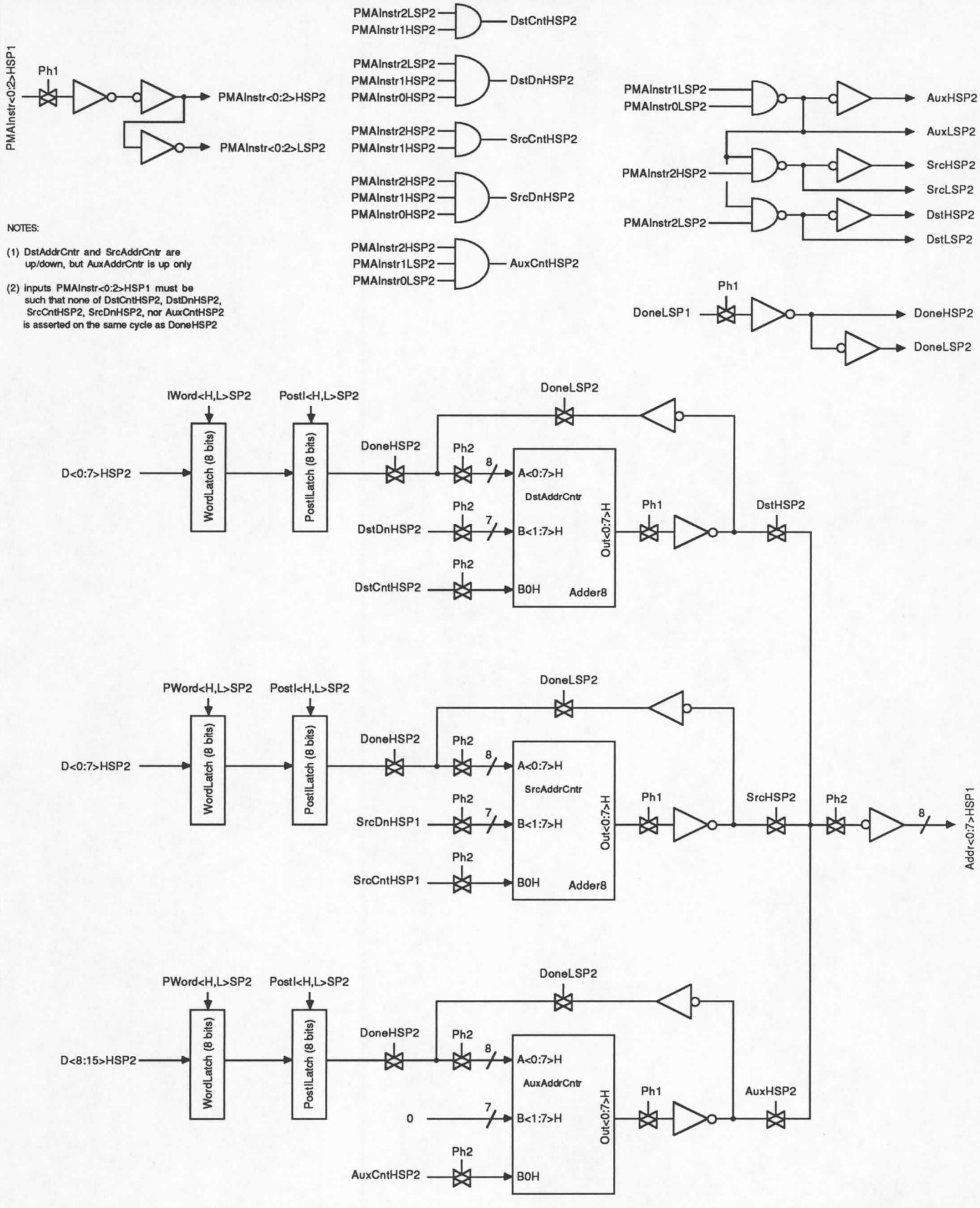


Incrementer cell of Sub-module AddrGen

Cells in Sub-module AddrGen of Sequencer

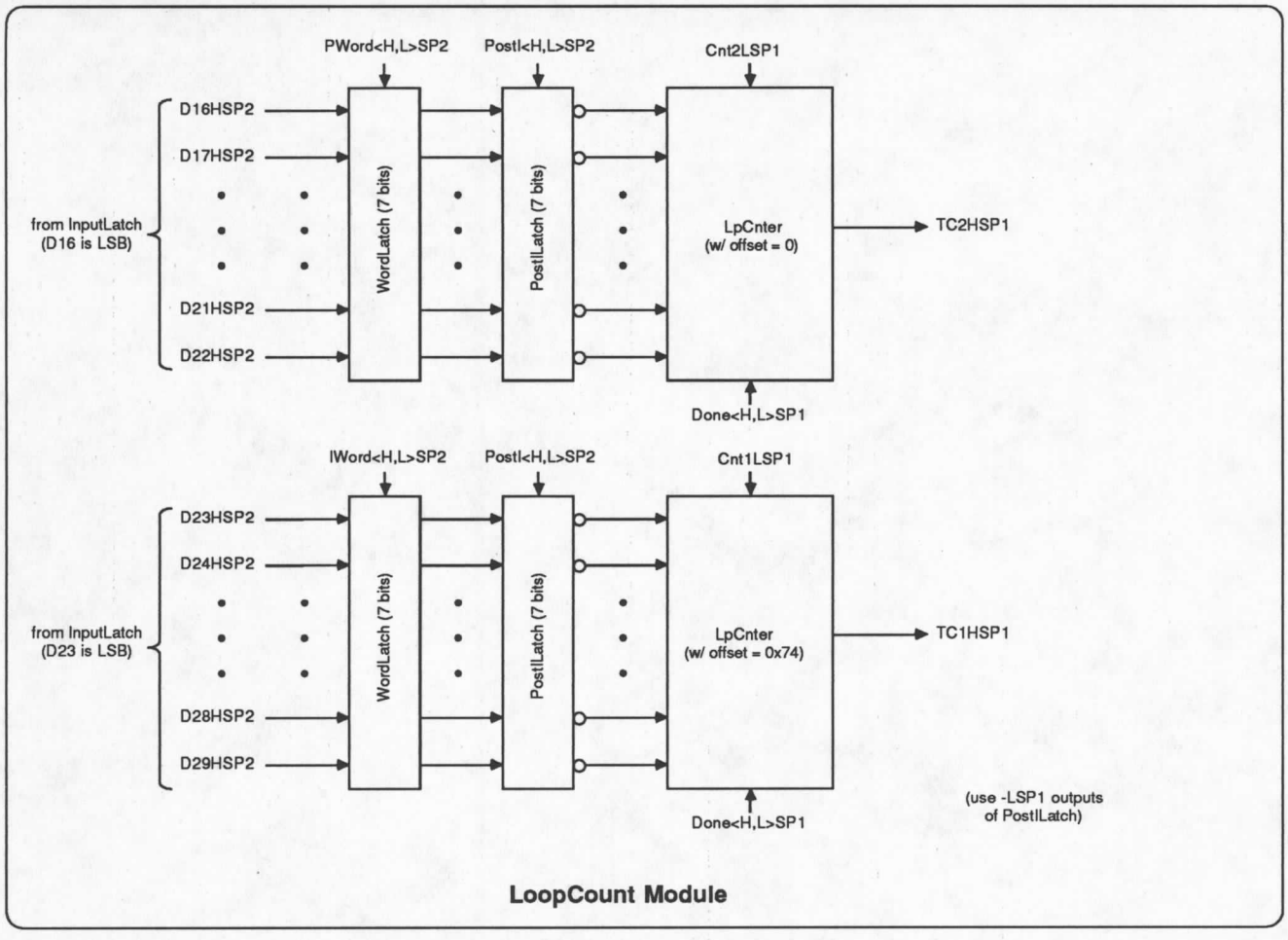


Memory sub-module of Sequencer

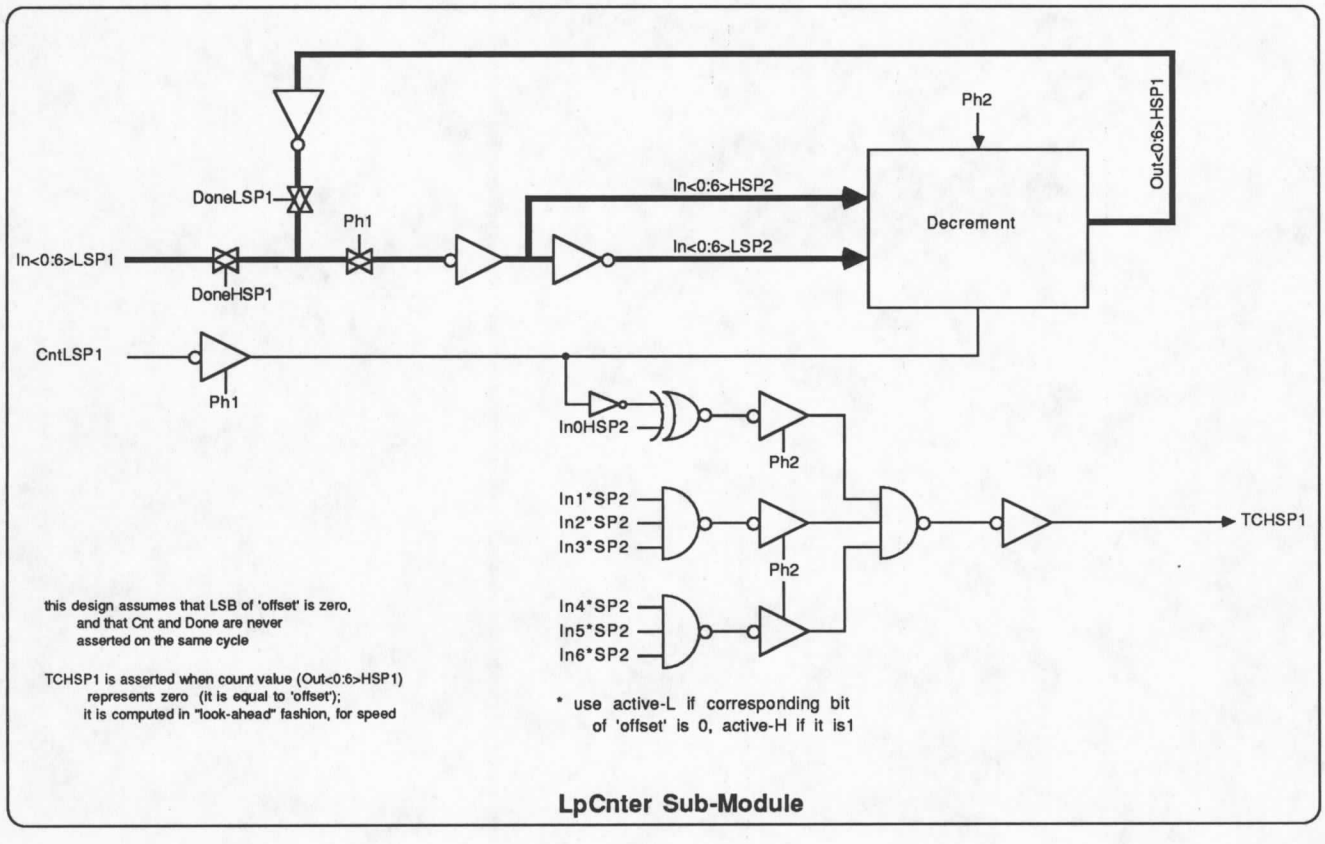


Block Diagram of PixMemAddr Module

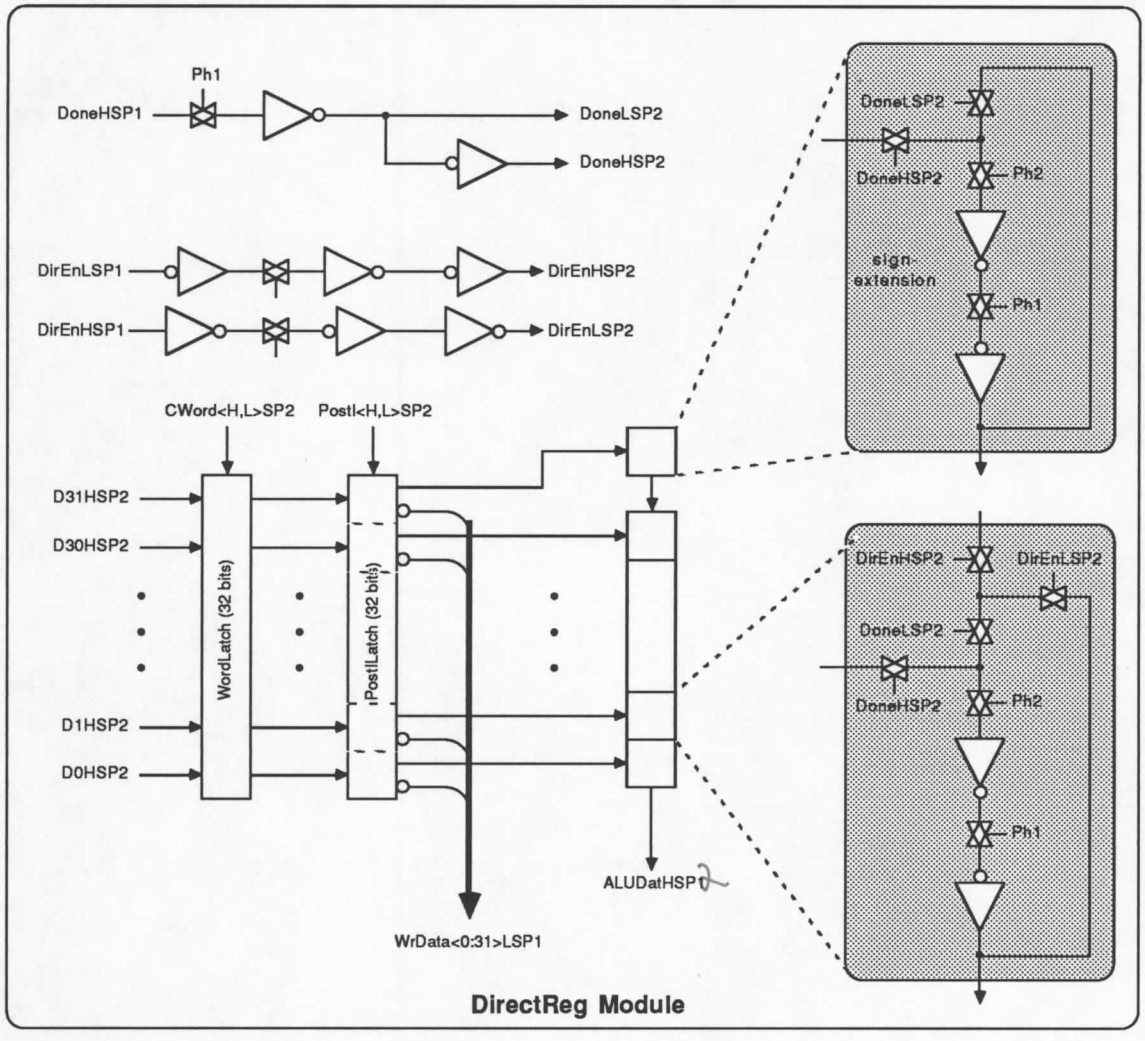
jge/7-Jun-89



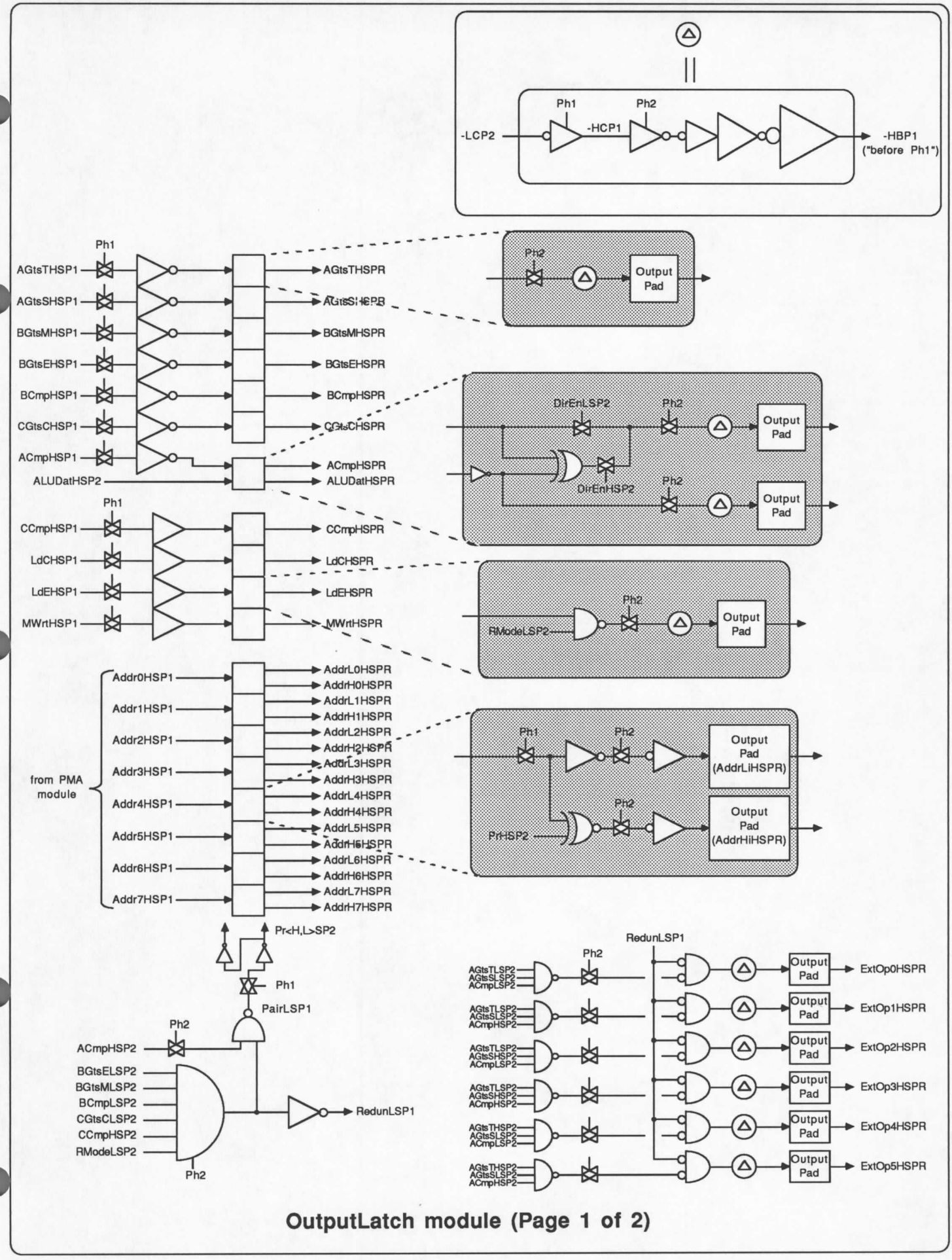
LoopCount Module



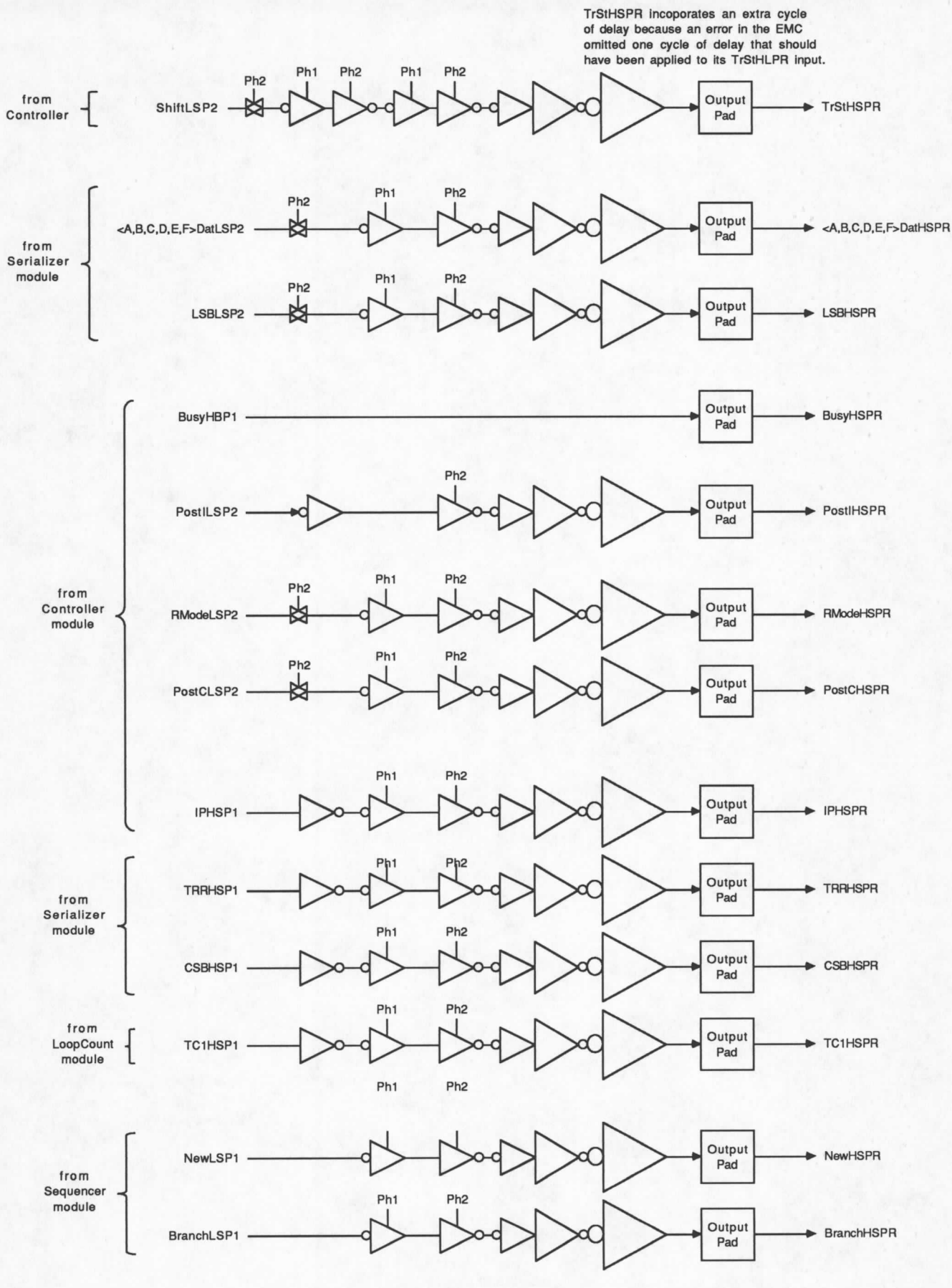
LpCnter Sub-Module



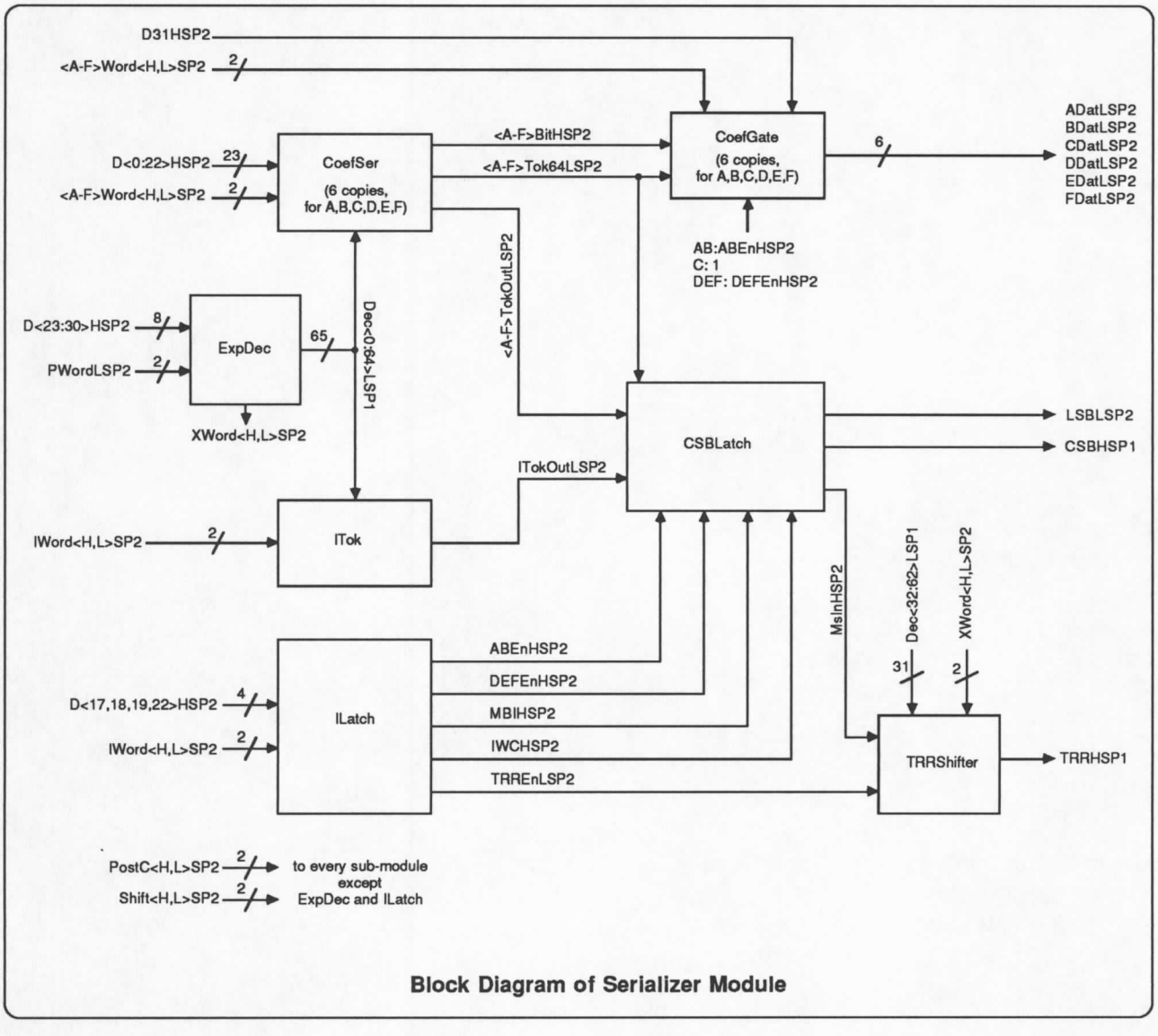
DirectReg Module



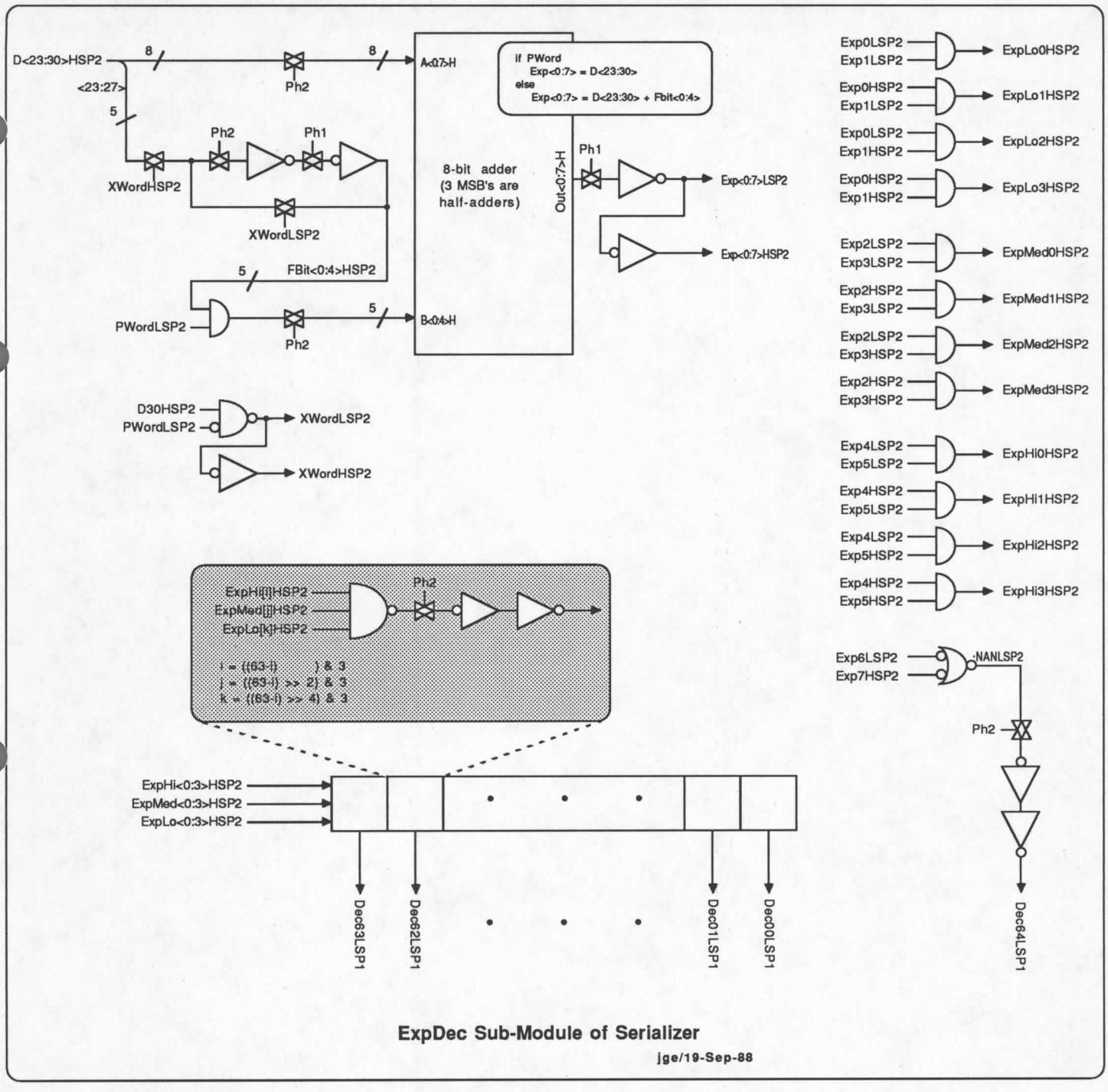
OutputLatch module (Page 1 of 2)



OutputLatch module (Page 2 of 2)

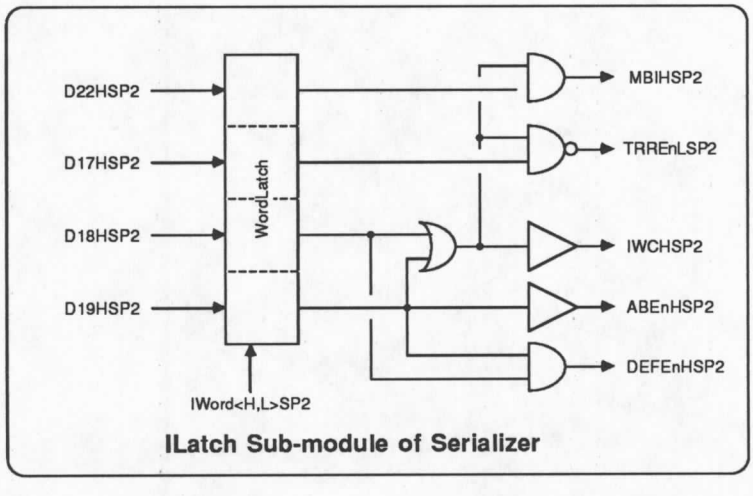


Block Diagram of Serializer Module

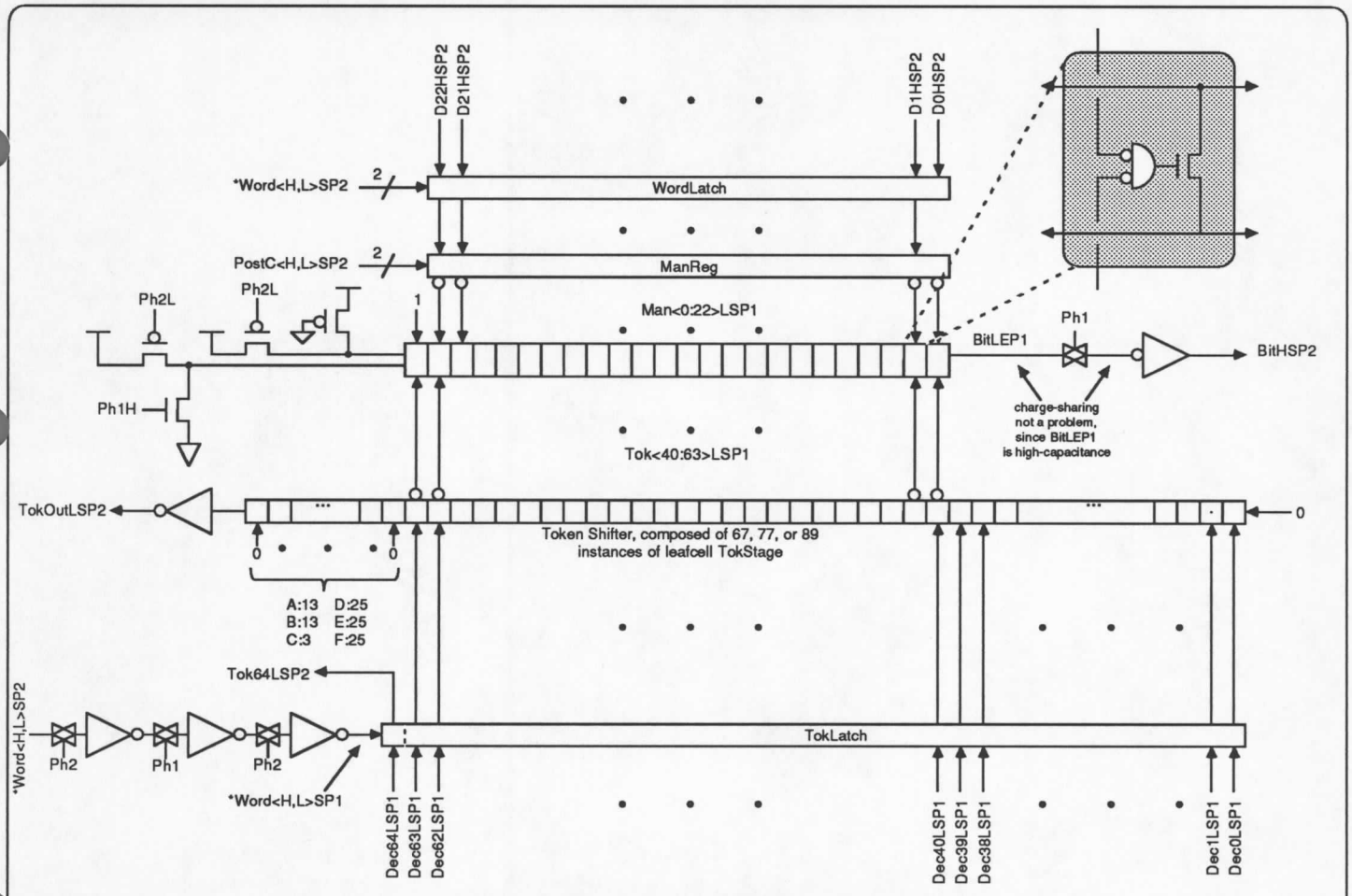


ExpDec Sub-Module of Serializer

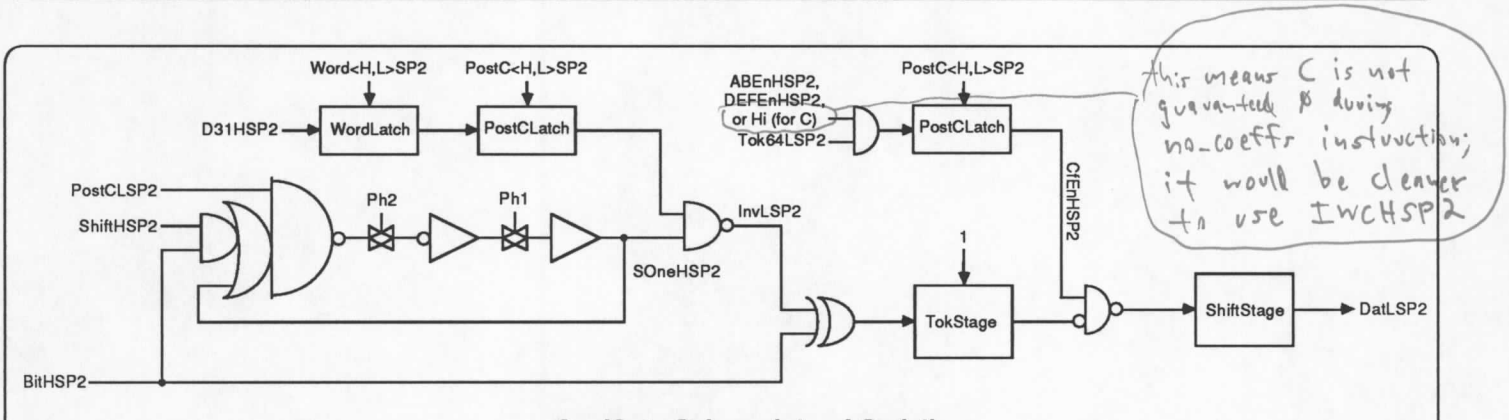
jge/19-Sep-88



ILatch Sub-module of Serializer

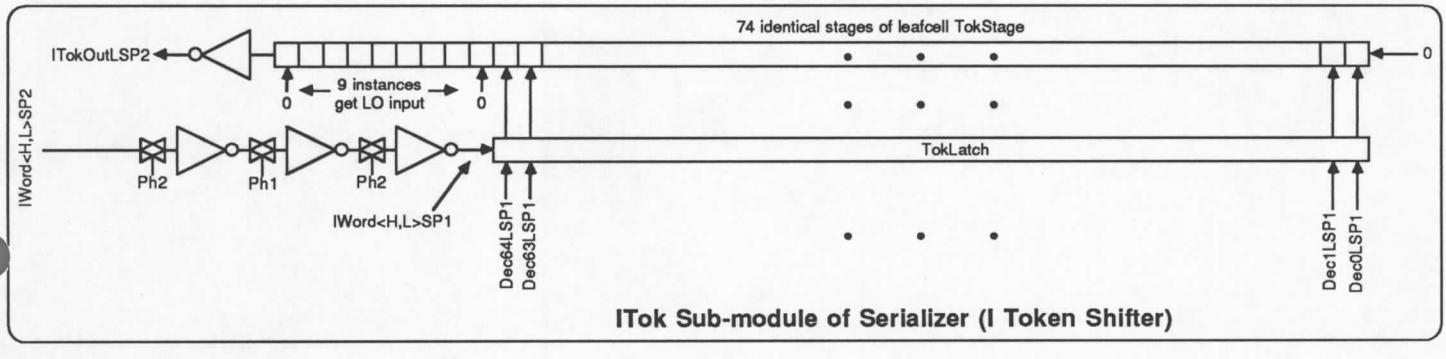


CoefSer (Coefficient Serializer) Sub-module of Serializer
(6 instances, one for each of A,B,C,D,E,F)

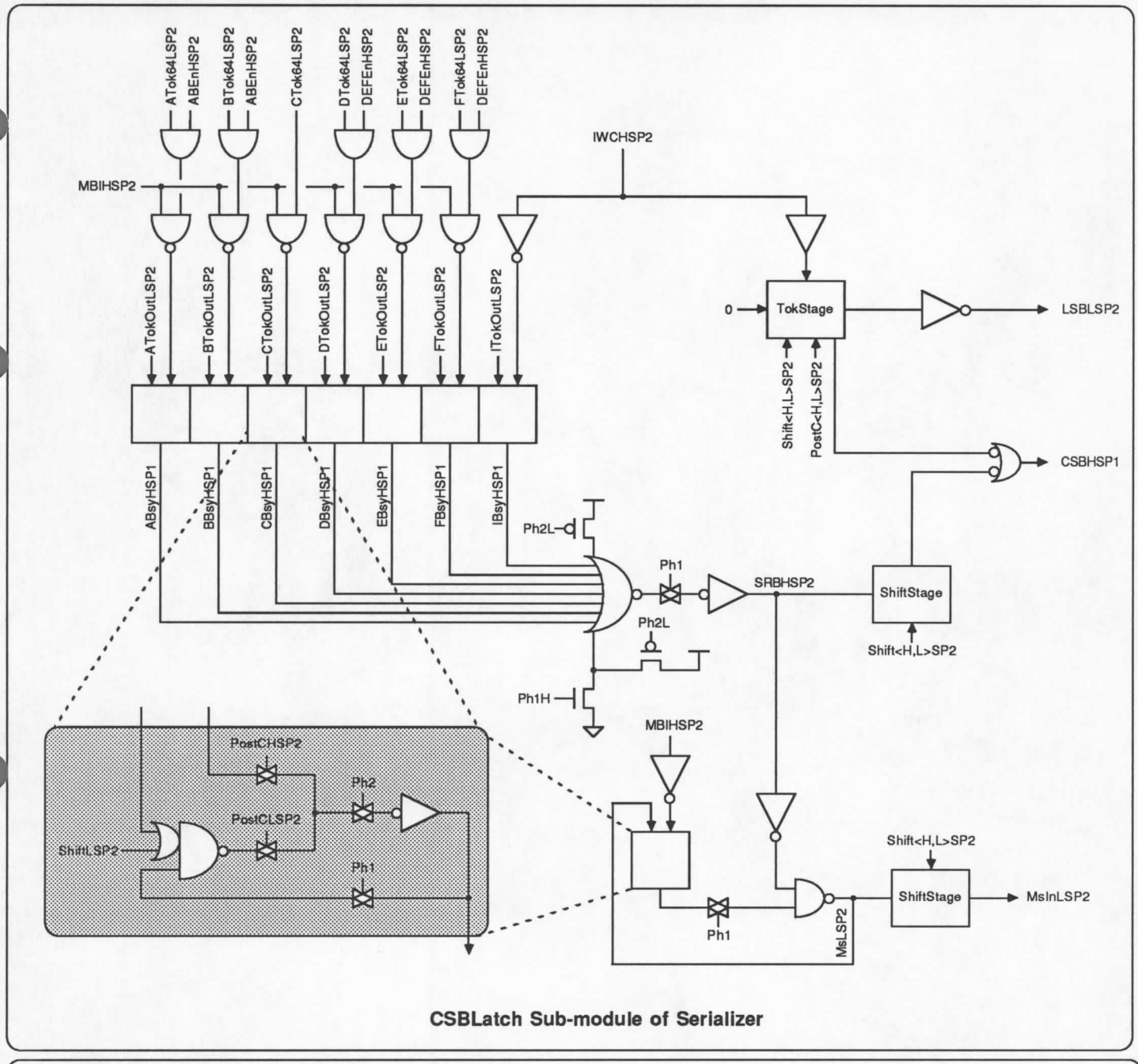


This means C is not guaranteed 0 during no_coeffs instruction; it would be cleaner to use IWCHSP2

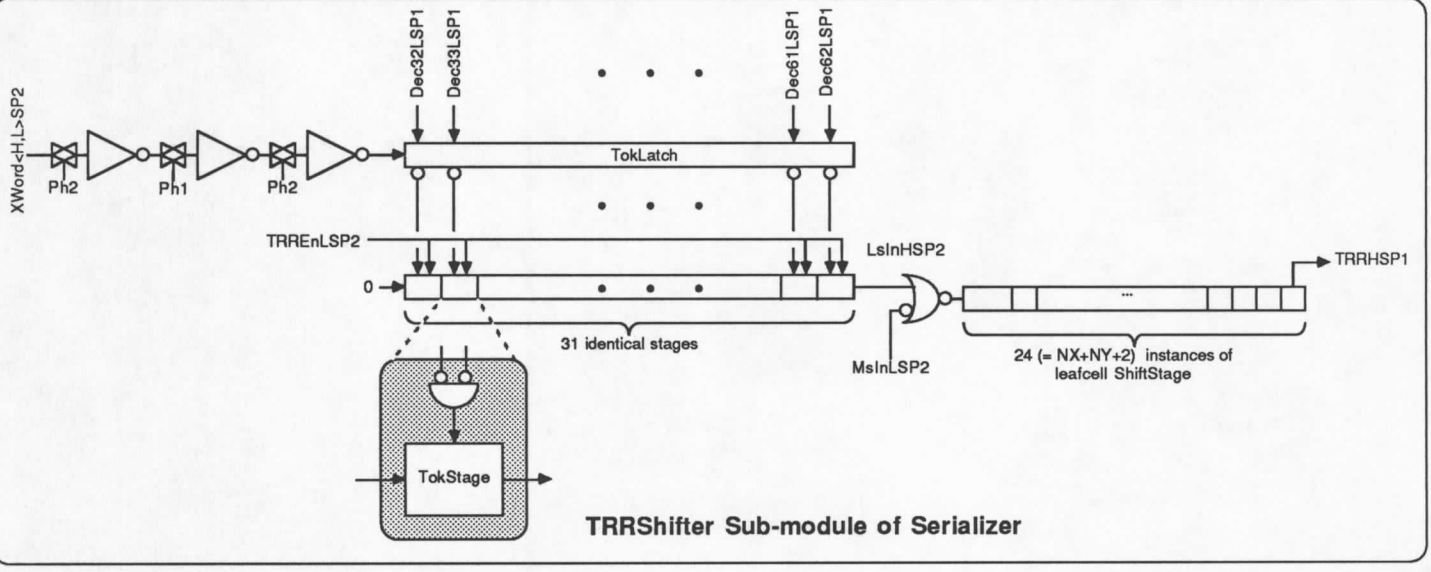
CoefGate Sub-module of Serializer
(6 instances, one for each of A,B,C,D,E,F)



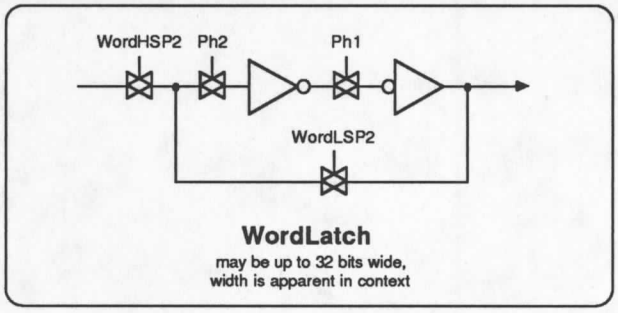
ITok Sub-module of Serializer (I Token Shifter)



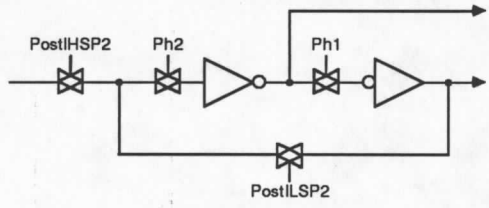
CSBLatch Sub-module of Serializer



TRRShifter Sub-module of Serializer

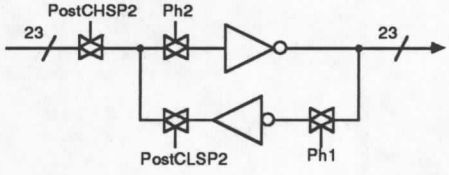


WordLatch
may be up to 32 bits wide,
width is apparent in context

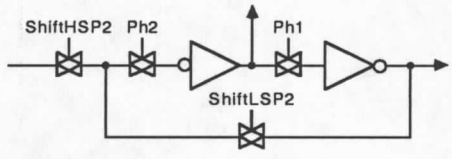


PostILatch
may be up to 32 bits wide,
width is apparent in context

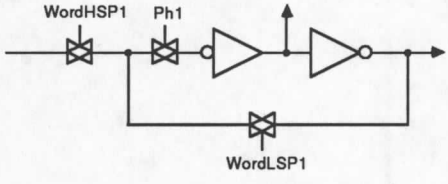
Commonly Used Leaf Cells in Most Modules



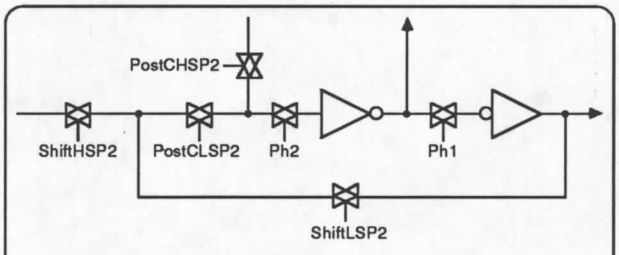
ManReg
23 bits wide



ShiftStage

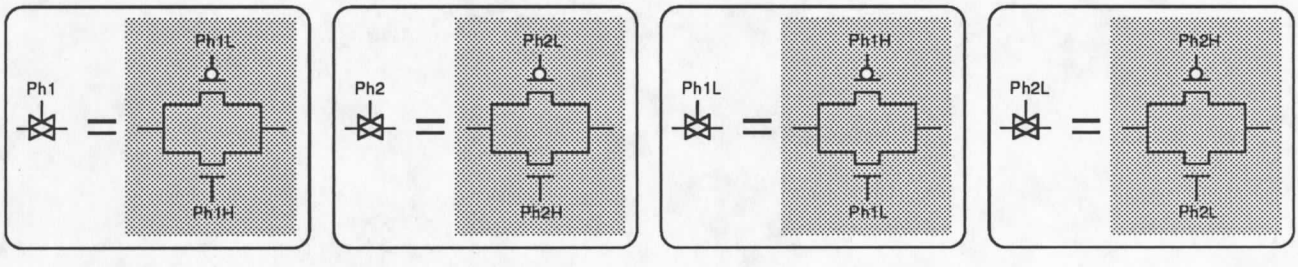


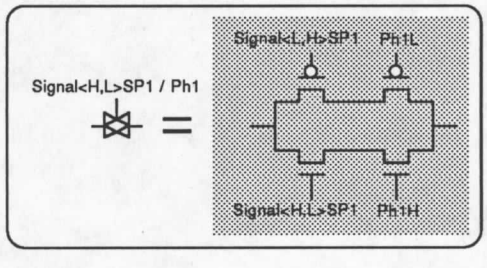
TokLatch
65 bits wide (except 31 bits wide in TRRShifter)

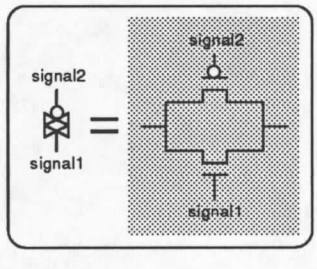


TokStage

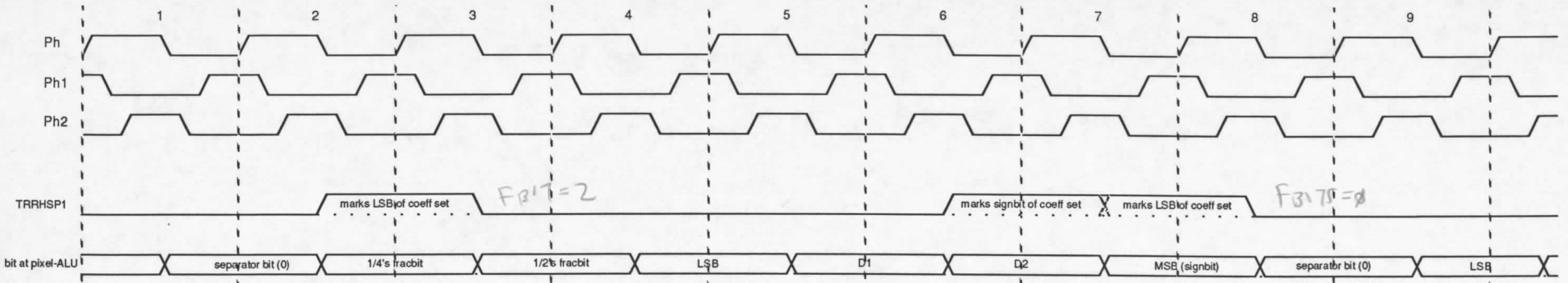
Commonly Used Leaf Cells in Serializer Module





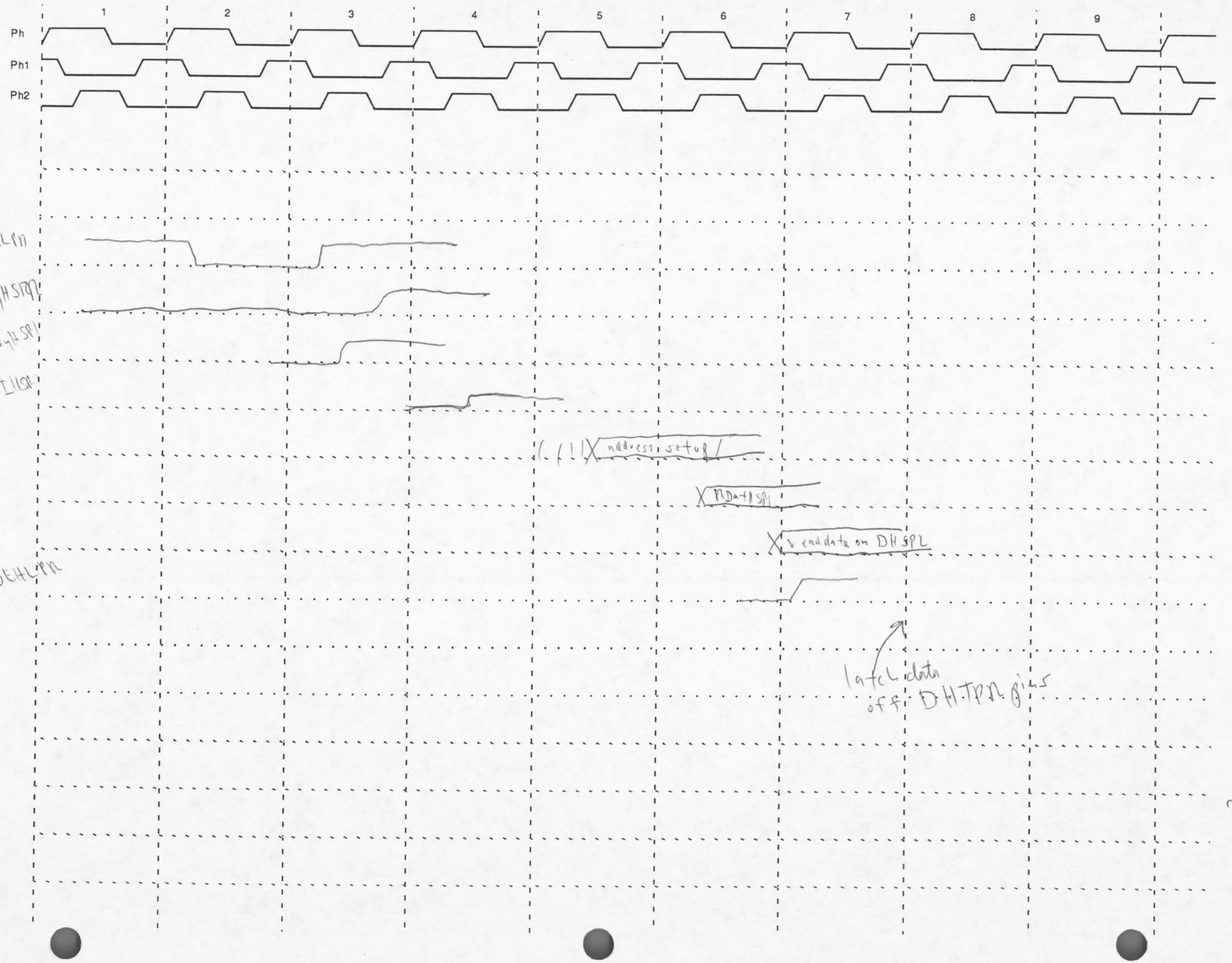


Circuit Abbreviations


1
2
3
4
5
6
7
8
9
Ph
Ph1
Ph2
TRRHSP1
marks LSB of coeff set
marks signbit of coeff set
marks LSB of coeff set
bit at pixel-ALU
separator bit (0)
1/4's fracbit
1/2's fracbit
LSB
D1
D2
MSB (signbit)
separator bit (0)
LSB

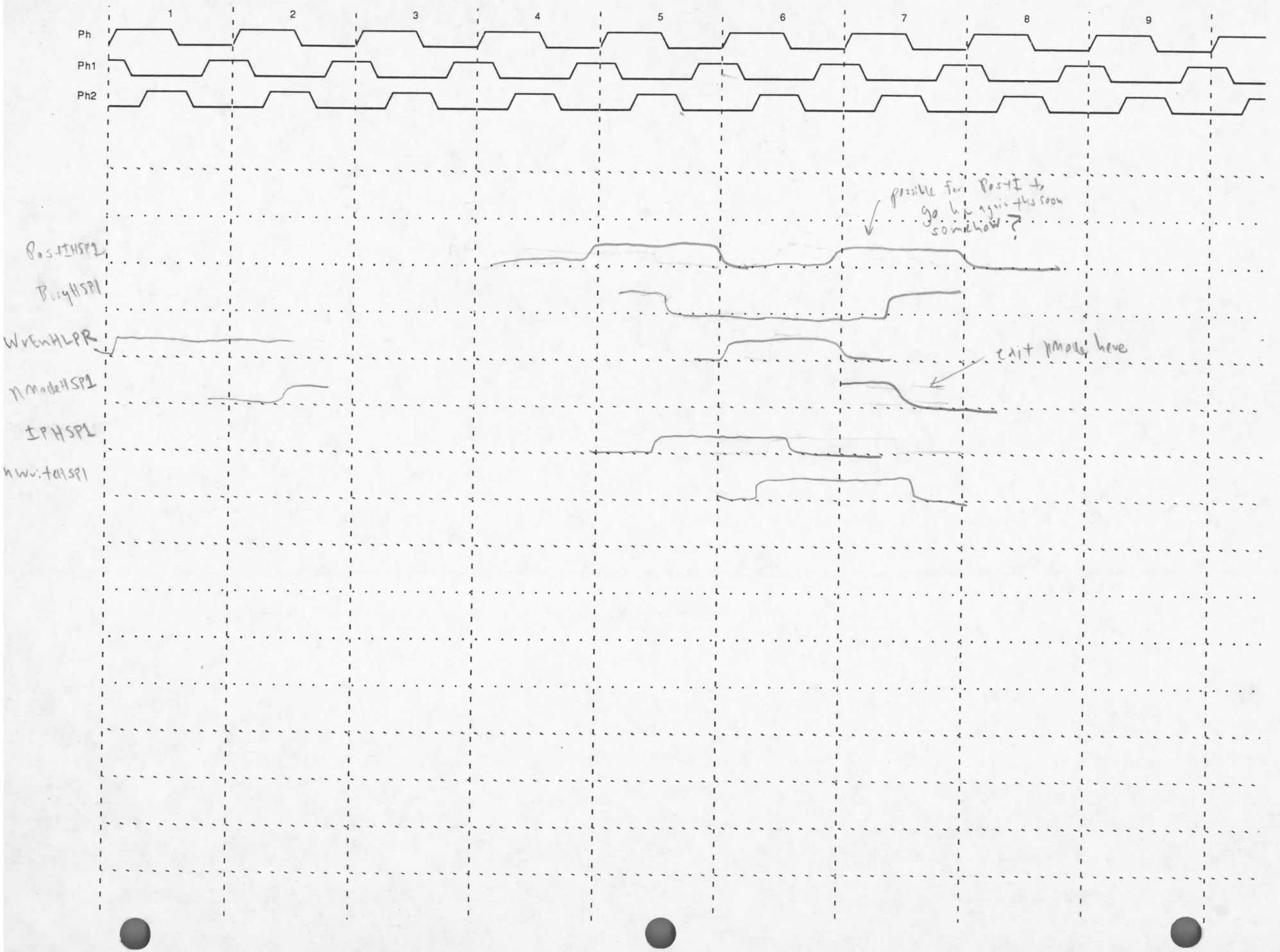

Timing of CSBHSP/CSD & Coeff Bits
1
2
3
4
5
6
7
8
9
Ph
Ph1
Ph2
PostCHSP1
LSBHSP1
CSBHSP1
DatHSP1
MSB
LSB
MSB
LSB
MSB
LSB

Test Mode (Reading Microcod Store)

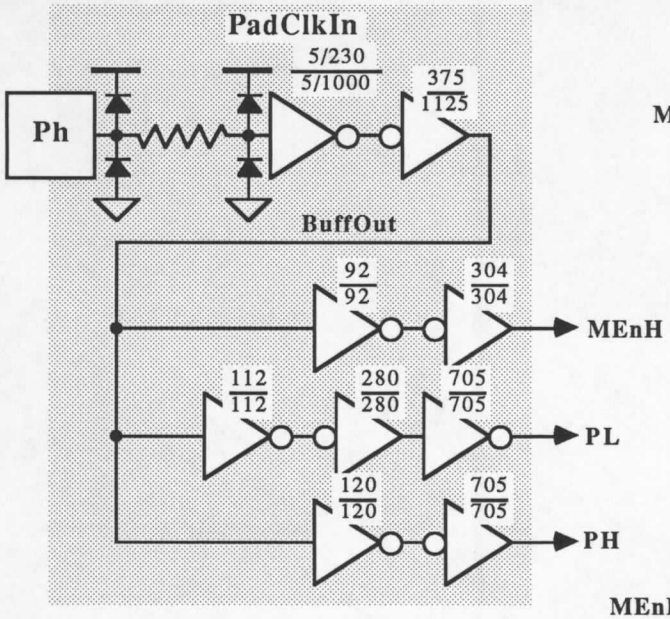


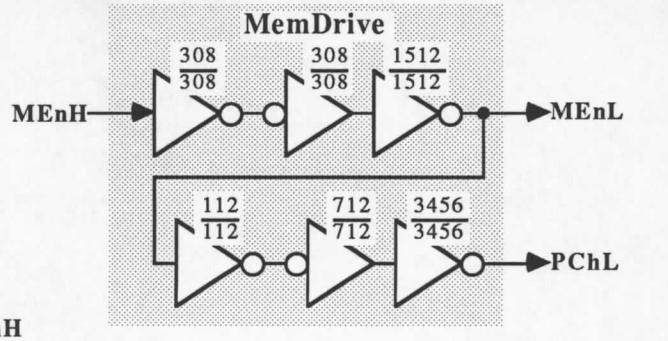
INPUT INTERFACE TIMING

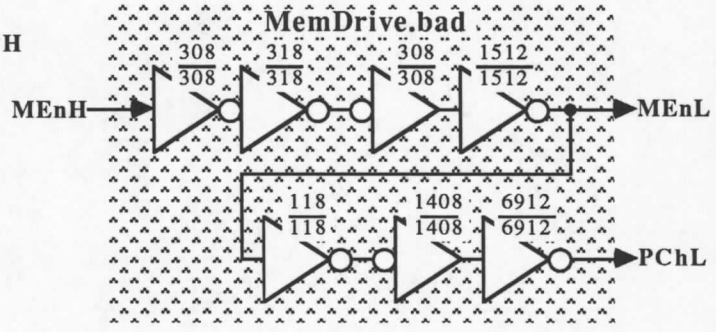
Write Cycle Timing (i-Mode)

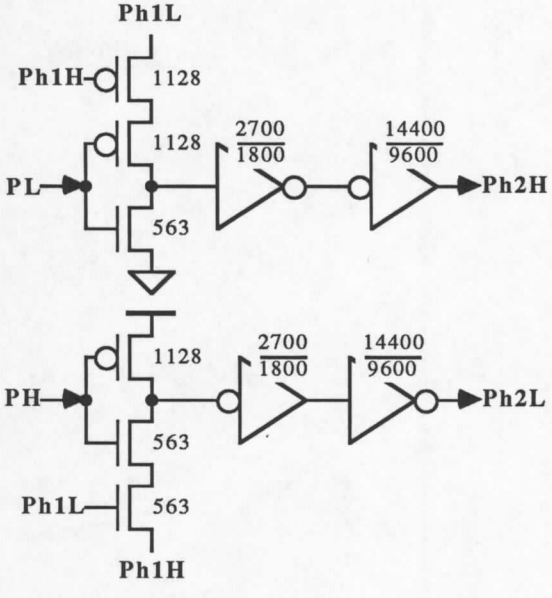


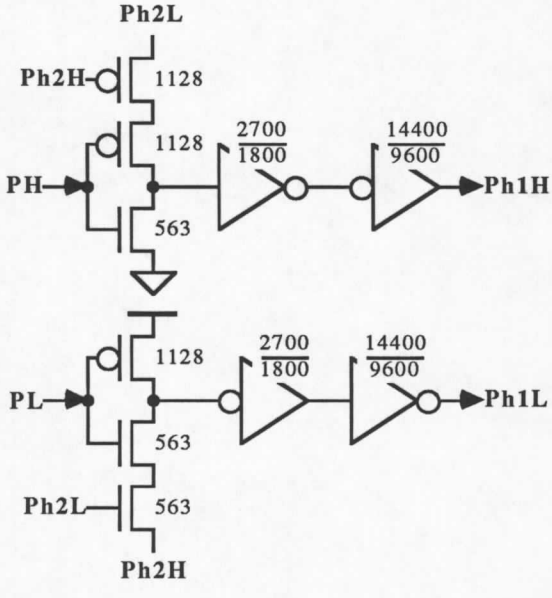
use add to IBC Pads











Note:
Transistor sizes in Lambda.

Pixel-planes 5

Project:	Pxpl5 IGC
Cell Name:	ClkGen
Dirs:	~jp/pxpl/igc/clkgen
Revision:	0-01 12 - 7 - 89 jp