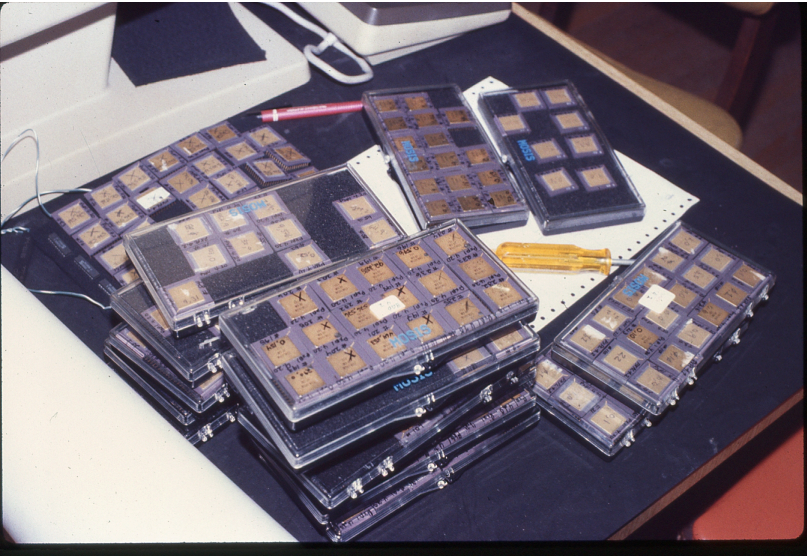


## OUR TESTING NEEDS:

- need 2000+ working, burned-in parts
- must fab 8000-10000 die
- must do wafer probing to avoid packaging bad parts at $25 each
- decision: do testing ourselves to avoid expense and headaches of interfacing with vendor
- testing must be:

  at or near operating speed

  minimal parametrics required

  UNIX-based

  quick and semi-automatic

## PREVIOUSLY AVAILABLE TESTERS:

### ACADEMIC:

not broadside

quite slow (50-200 KHz)

### PRODUCTION TESTERS:

very high through-put

comprehensive parametrics

very expensive ($ 0.5-2 million)

### LOGIC-ANALYZER BASED:

affordable

intermediate performance

difficult to interface with UNIX
(IEEE-488 , too slow)

**Hewlett-Packard 8180**

50 MHz; 192 pins; 1Kbit/pin
$1.7K / channel
PG only--company sells compatible SA

**Hilevel Technology PG3700**

50MHz; 512 pins; 1,4,or 16 Kbit/pin
$800 / channel
500 ps edge placement
Adjustable output voltages, many data formats

**Integrated Measurement Systems (IMS)**
**Logic Master I**

20 MHz; 432 pins; 8Kbit/pin
$460 / channel, controlled impedance test head
General-purpose translator for various workstations
Many data formats (NRZ, RZ, R1, DNRZ) on 48 ch's
DC parametric measurement unit available

**Logic Master II**

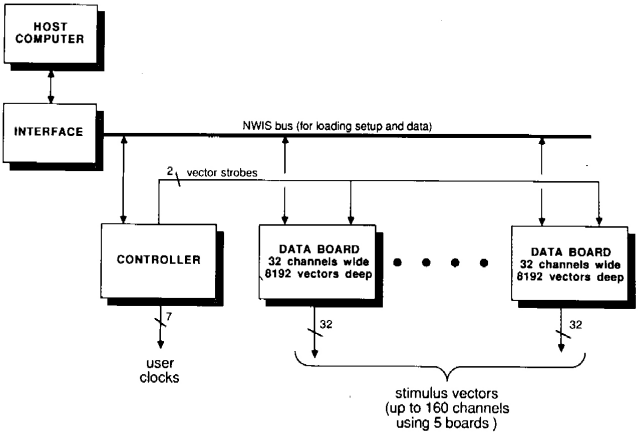
Same as LM I, except:
16Kbit/pin, 1ns edge placement
$650 / channel
Adjustable output levels

**Northwest Instrument Systems 2300**

20 MHz (7 ch's-100MHz), 160 pins, 4Kbit/pin
$330 / channel
NRZ only, 2ns edge placement

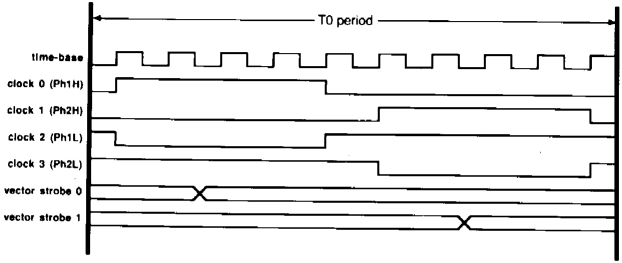
**Tektronix 91S32 & 91P32**

25 MHz, 80 pins, 1Kbit/pin
$520 / channel (S32); $415 / channel (P32)
Adjustable output levels on S32

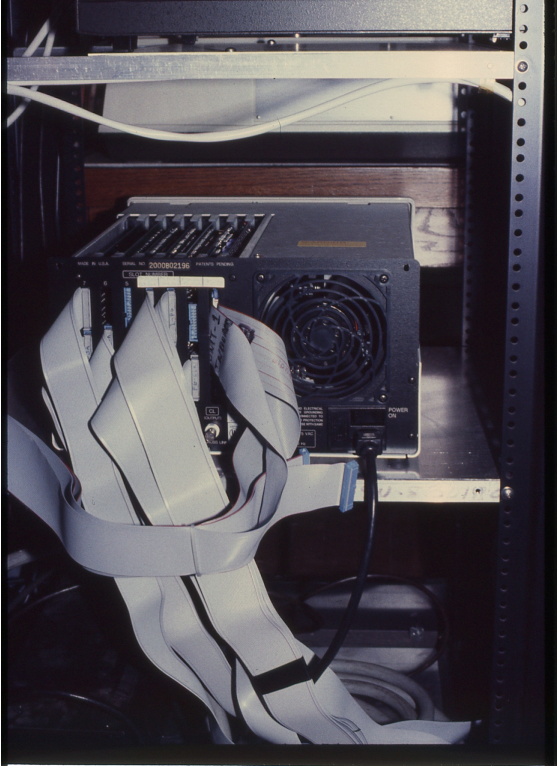


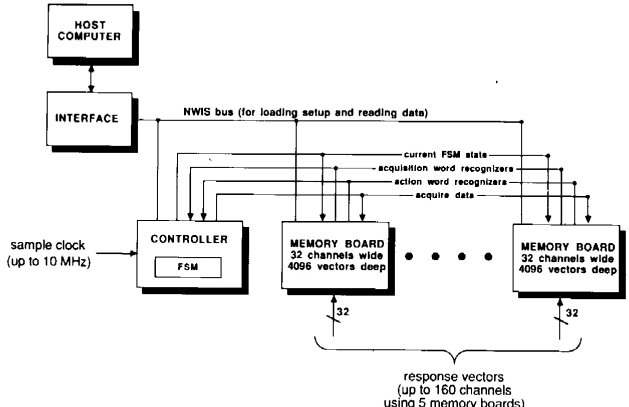

# Pattern Generator

## Programming the NWIS Pattern Generator




- select timebase: 10,20,...,160 nanosec or external
- select length of T0 period as 4 to 250 timebase cycles (normally, T0 period would correspond to clock cycle of DUT)
- program user clocks and vector strobes using time-base granularity
- offset edges of clocks and strobes in 2 ns increments using tapped delay lines
- load test vectors, including tri-state enables, into 32-channel data boards
- assign a vector strobe to each 32-channel data board
- load starting vector number and repeat vector number into data boards
- go


MADE IN U.S.A.
SERIAL NO. 2000802196
PATENTS PENDING
POWER
ON




State Analyzer

## Programming the NWIS State Analyzer

program the word recognizer RAM's on each 32-channel memory board; these cause the various 'acquisition word recognizer' and 'action word recognizer' lines to be asserted based on the values of the current response vector

program the finite state machine on the controller board; the 'action word recognizer' lines control branching among the 16 states of the FSM

in each state, the acquisition of the current response vector is defined according to the values of the 'acquisition word recognizer' lines

## For Our Application

the full capability of the FSM, which allows versatility equivalent to standard logic analyzers, was not necessary for our application

instead, we program the FSM to simply initialize at state 0 and remain there until the machine is halted

we program the acquisition word recognizers to store the response vector whenever a pre-designated input bit is 1; this input bit is connected to one of the pattern generator signals which is dedicated as 'acquisition enable'

Limitations of NWIS Pattern Generator:

no algorithmic pattern generation capability

no control of rise and fall times for patterns or clocks

no control of high and low logic levels

signals can be tri-stated only by bytes, not per pin

active edges of vector strobes must be separated by minimum 50 ns (maximum vector rate = 20 MHz)

all signals are NRZ (non-return to zero), that is, each signal is either high, low, or high-Z from one vector strobe until the next vector strobe

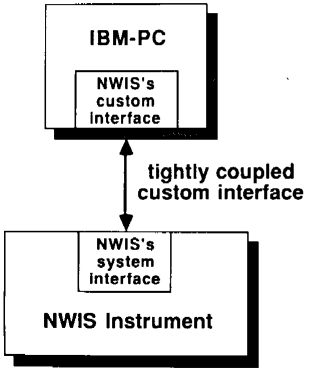
all 32 channels on one data board are strobed in unison, as defined by the vector strobe enabled on that board

no mechanism for trading off pattern depth versus pattern width

maximum pattern width is 160 channels

maximum pattern depth is 8192 vectors (should be upgraded to 32k soon)

## NWIS APPROACH




## PROBLEMS

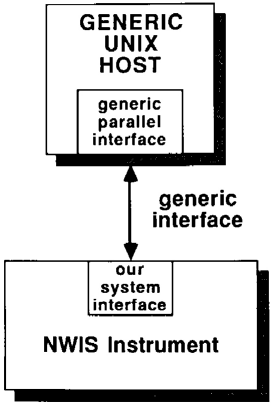
interface is tightly integrated into driver software

therefore not readily portable to other hosts

IBM-PC running MS-DOS is not suitable for integrated design - manufacture - test cycle

not feasible to bring test patterns from UNIX machine to PC

## OUR APPROACH




## ADVANTAGES

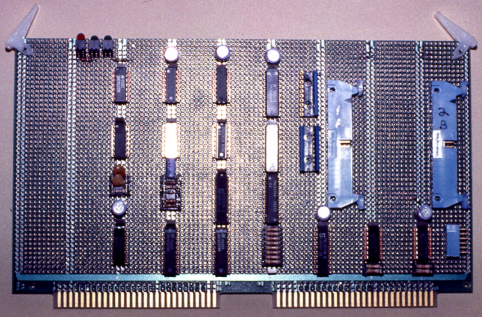
NWIS now lives on industry standard DR-11 interface

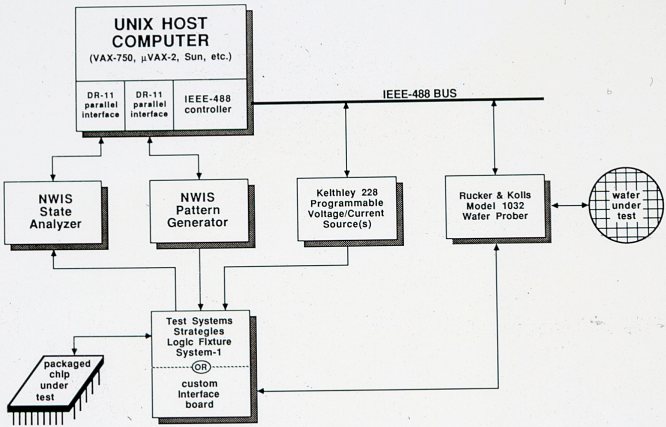
thus can be tightly coupled to UNIX machines where IC design files live

can control NWIS, wafer prober, power supplies, etc. from UNIX

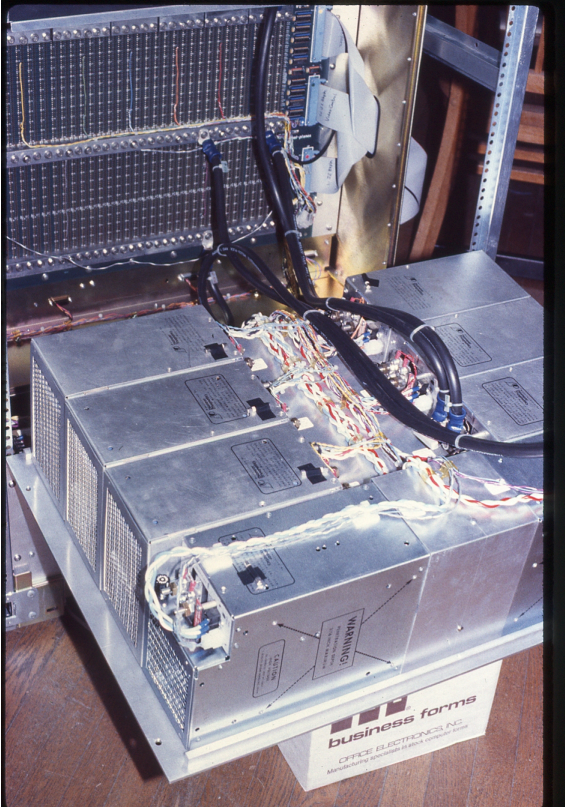
## DISADVANTAGE

discarded NWIS's very nice interactive menus






UNIX-NWIS Tester


WARNING
business forms
OFFICE ELECTRONICS, INC.

Test Program:

1) set-up State Analyzer

2) set-up clock discipline on Pattern Generator

3) get test vectors off disk, download to Pattern Generator

4) put all pins in test fixture to GND potential

5) prompt user to insert chip, enter its number

6) arm State Analyzer and Pattern Generator and de-assert Master Halt signal

7) wait for test to complete

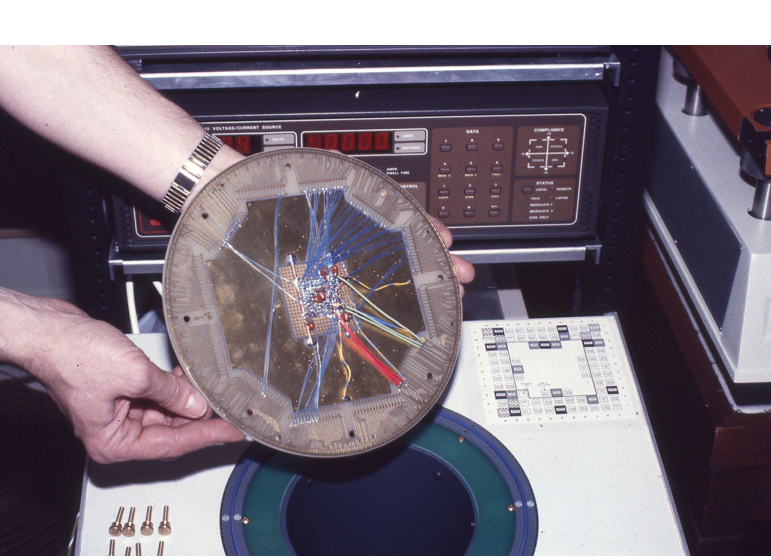
8) put all pins at GND potential

9) prompt user to change chip

10) upload response vectors from State Analyzer

11) analyze response vectors, write files onto disk

12) go to Step 6


VOLTAGE/CURRENT SOURCE
DATA
COMPLIANCE
STATUS


LFS-1

# COST (not incl. wafer probing):

## Monetary: (not including host computer)

| | |
|---|---|
| Pattern Generator (96 channels) | $17450 |
| State Analyzer (96 channels) | 9025 |
| Test Head | 7200 |
| Load Boards for Test Head (5) | 750 |
| Programmable Power Supplies (2) | 7000 |
| Parallel Interface Boards (2) | 700 |
| IEEE Bus Controller | 2000 |
| | $44125 |

## Engineering Time:

| | |
|---|---|
| Systems Programming (drivers for parallel interfaces and IEEE-488 controller) | 1 man-month |
| Porting NWIS code to UNIX | 2 man-months |
| Additional UNIX applications code | 1 man-month |
| Construction of rack | 2 man-days |
| Customizing each load board | 0.5 man-days |